EBConverter V1.3TM Do Quick! Done Right! Protect Your IP!

EBConverter V1.3[™] provides a solution for converting Cadence Allegro[™] Layout board to IBIS EBD Industry Standard Modeling Format (<u>http://www.eigroup.org/ibis</u>).

Many module vendors deliver their board designs to their customers for the high-speed system designs. There are risks for their IP protections as well as tool interoperability issues. IBIS EBD provides a standard (ANSI/EIA) modeling format to allow module vendors deliver the standard modeling format to their customers as well as protecting their IP in the module designs.

EBConverter V1.3[™] is the most accurate EBD converter tool on the market. It automatically uses the embedded terminator solution in the EBD to provide complete extended netlist and generates IBIS Terminator models with power/ground connections according to the connections in the layout board.

Package Pin (Connection (4 Pin)		×		
Name:	4PIN_ISOLATED_				
Net< ≻	RefDes . Pin Name	Pair Pin			
	DQ7 < ≻ RN3 . 1	4	~		
	DQ3 < > RN3 . 2	3	~		
	DQ3A < > RN3.3	2	~		
	DQ7A < ≻ RN3 . 4	1	~		
		🔲 Bussec	I		
	Apply	Cancel			

- Auto-Mapping capabilities
- Project save / load functionalities

[DML File]	Load DML									
[Save Path]	C:\IOMETH\SRC\EBConverteritest\testcase\				Save Path				Met	ĥ
[Project File]	C:VOMET	H\SRC\EBC	onverterN	est\testcase\u	ı-dimm_	Load Pr	oject	Conne	ctor Device	 ,
[File Name]	u-dimm_	_rcc	. ebd	[File Rev]	1.0			J1		•
[Notes]										
Converted	from DML	BoardMode					*		nformation	
Device Mod	el Mapping	9								
	C29 C30 C31 C32 C33 C34 C35 C36				c29.il c30.il c31.il c32.il c33.il c34.il c35.il c36.il		CAP_0 CAP_0	603_1_SPF 603_1_SPF 603_1_SPF 603_1_SPF 603_1_SPF "CAP_ "CAP_	25PF 25PF	* •
IBIS File Na	or Setting	Resistance		. ibs IBIS C Capacita	omp Nar	ne Farad	Pin Cor	nnections	Set	
				estitestcase\u estitestcase\u				. Loaded		* *
About EBC	onverter		Help		Save P	oject	CON	VERT	Qui	t

EBConverter V1.3[™] provides:

- Flexible Connect Device (Connector) selection
- Complete Connector Pin list

• Automatic serial/parallel terminator handling for complete extended netlist

• Automatic embedded terminations in [Path Description] and IBIS Terminator model generations

• Support Cadence PCB SI Detailed Closed Form Via Modeling

• Keep all the data name (Net, RefDes, etc.) as the same as original board

• Remain DML boardmodel segment names as comments for easy verification

• Terminator Pin Setting Wizard with automatic Net detecting

