
Deliver your EBD model with confidence

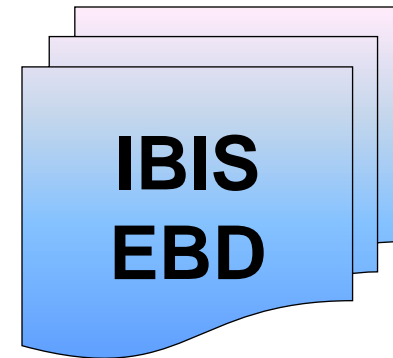
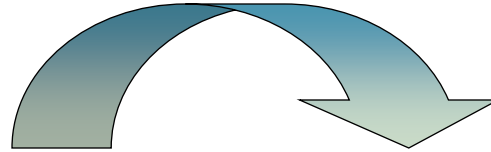
EBCConverter V1.2™

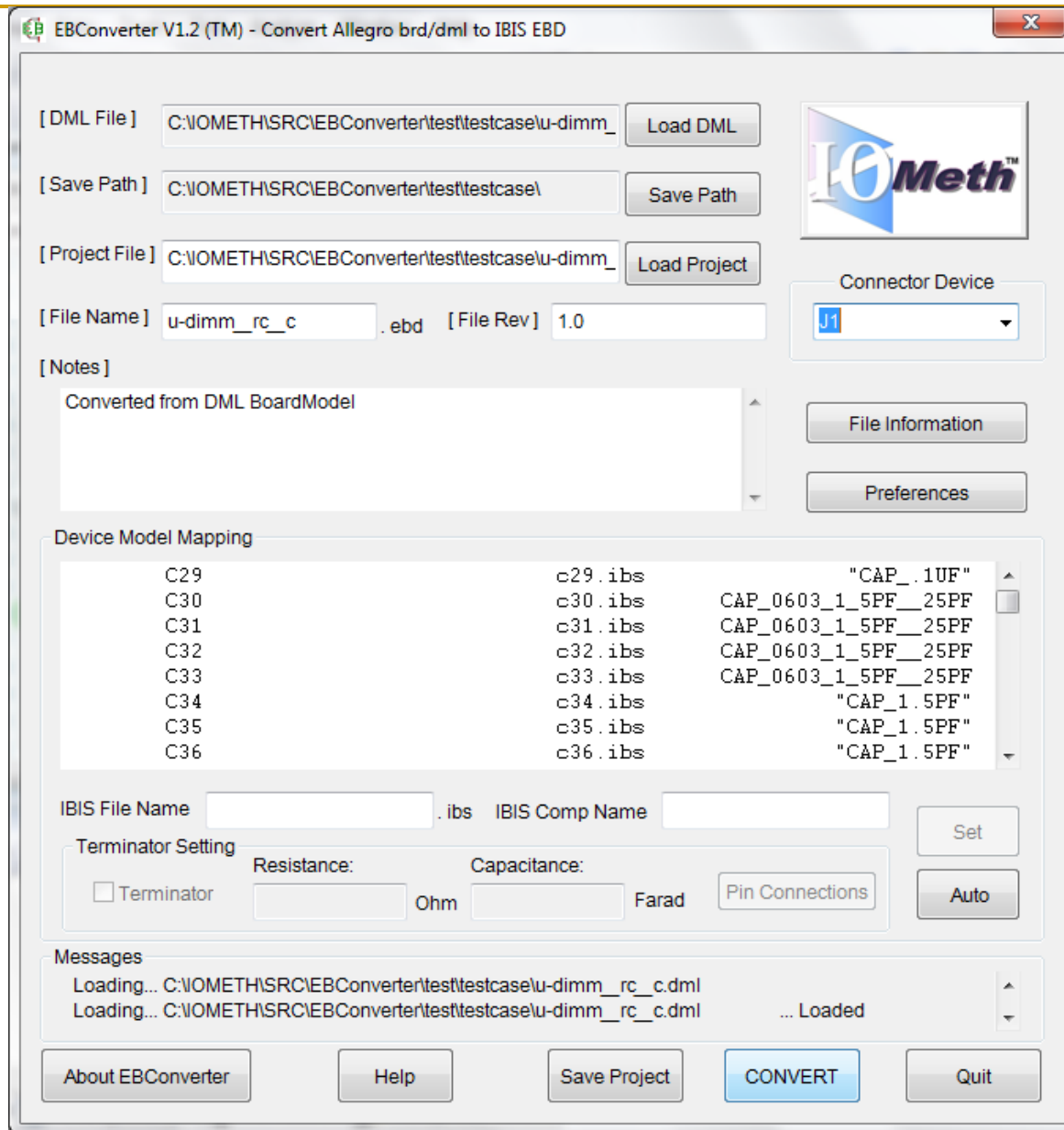
Release 201104



EBConverter V1.2™

- Convert your Allegro brd / dml to IBIS EBD model

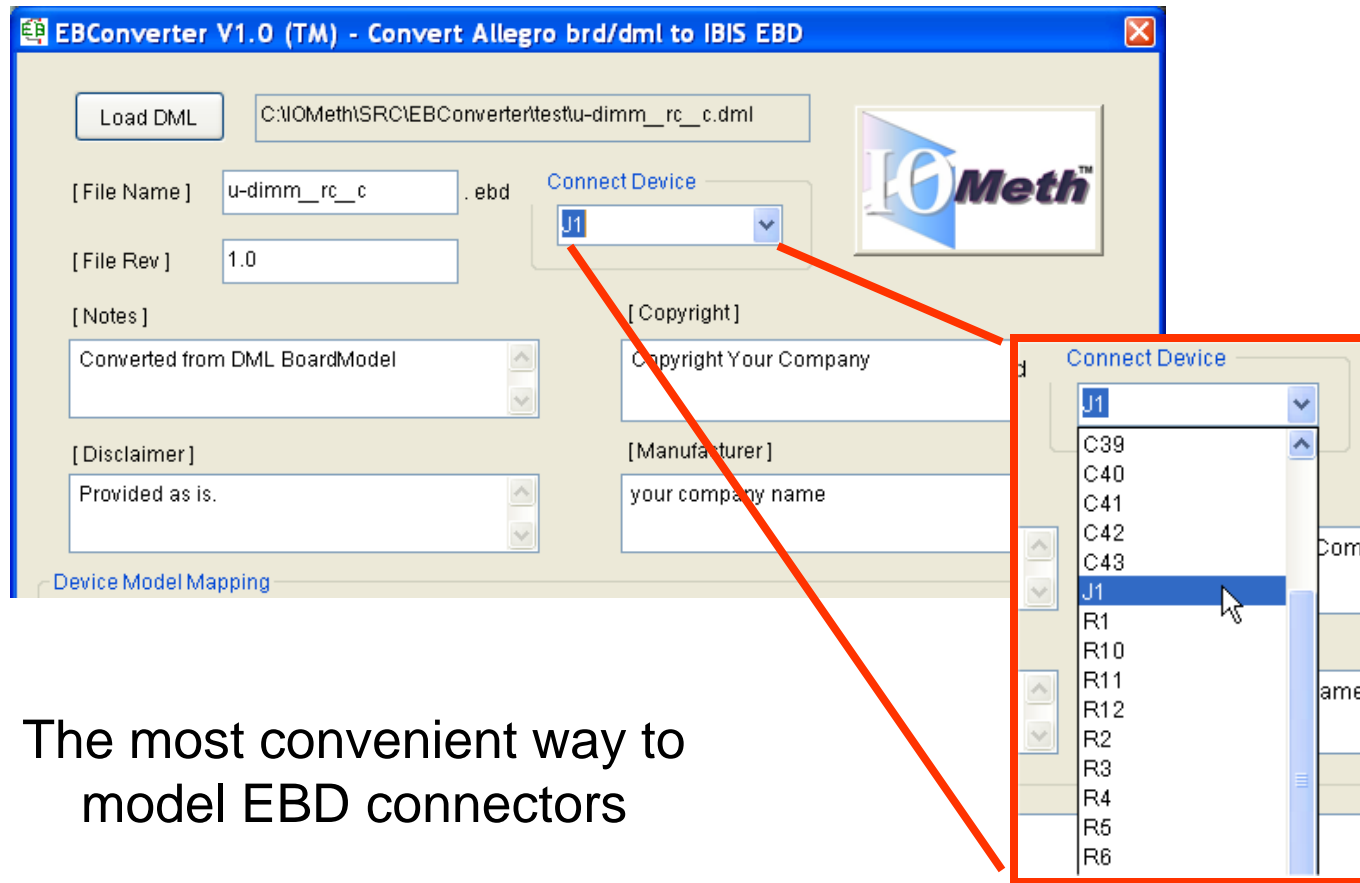




EBConverter V1.2™

- The most accurate IBIS EBD converter on the Market
 - Flexible Connect Device (Connector) selection
 - Complete Connector Pin list
 - Automatic serial/parallel terminator handling for complete extended netlist
 - Auto-mapping capability for terminator mapping
 - Automatic embedded terminations in [Path Description] and IBIS Terminator model generations
 - Keep all the data name (Net, RefDes, etc.) as the same as original board
 - Optional remained DML boardmodel segment names as comments for easy verification

Flexible Connect Device (Connector) Selection



The most convenient way to model EBD connectors

Complete Connector Pin list

```
[Number Of Pins] 184
```

```
[Pin List] signal_name
```

```
| J1.1  
1 POWER  
| J1.2  
2 DQ0  
| J1.3  
3 GND  
| J1.4  
4 DQ1  
| J1.5  
5 DQSO  
| J1.6  
6 DQ2  
| J1.7  
7 POWER  
| J1.8  
8 DQ3  
| J1.9  
9 NC  
| J1.10  
10 NC  
| J1.11  
11 GND  
| J1.12  
12 DQ8  
| J1.13  
13 DQ9  
| J1.14  
14 DQS1  
| J1.15  
15 POWER
```

```
| J1.173  
173 NC  
| J1.174  
174 DQ60  
| J1.175  
175 DQ61  
| J1.176  
176 GND  
| J1.177  
177 DM7  
| J1.178  
178 DQ62  
| J1.179  
179 DQ63  
| J1.180  
180 POWER  
| J1.181  
181 SA0  
| J1.182  
182 SA1  
| J1.183  
183 SA2  
| J1.184  
184 VDDSPD
```

Produced by another tool

```
[Number Of Pins] 172  
[Pin List] signal_name  
1 POWER  
2 DQ0  
3 GND  
4 DQ1  
5 DQSO  
6 DQ2  
7 POWER  
8 DQ3  
11 GND  
12 DQ8  
13 DQ9  
14 DQS1  
15 POWER  
16 CK1  
17 CK1#  
18 GND  
19 DQ10  
20 DQ11  
21 CKEO  
22 POWER  
23 DQ16  
24 DQ17  
25 DQS2
```

**Wrong Pin Mapping
with missing pins !!!**

Robust Terminator Handling

```
[Path Description] DQ0
| J1.2
Pin 2
| R@@X2130Yn370L1_@@J1.2
| ignored for Spice simulator
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/
| XNTL_XSTLX2350Y1370L1X4040Y5321L1
| Len=0 L=0.00382234 C=0.0000e+000 R=1.0000e-006/
| R@@X2350Y970L1_@@U1.1
| ignored for Spice simulator
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/
| RN1.1 -> RN1.8 R=22
| Len=0 R=22/
| Net: DQ0A
| R@@X2350Y1370L1_@@RN1.8
| ignored for Spice simulators
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/
| XNTL_XSTLX2350Y1370L1X4040Y5321L1
| Len=0 L=0.0145933 L=3.6466e-007 C=8.8655e-011 R=4.5129e+000/
| R@@X4040Y5321L1_@@U1.54
| ignored for Spice simulators
| Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/
Node U1.54
```

**Embedded termination
for extended netlist**

```
[Component] 2PIN_2GR100K
[Manufacturer] Created by EBConverter
```

```
[Package]
|-----|
| variable typ min max
[CompR_pkg 0 NA NA
[ManuL_pkg 0 NA NA
[C_pkg 0 NA NA
```

```
[Pack]
|
| [Pin] signal_name model_name
R_pkg [Pin] signal NC
L_pkg 1 signal term_p0_g0_rp_rg0
C_pkg [Series Pin Mapping] pin_2 model_name
| 1 2 series_r100K_c

[Pin]
1 signal NC
2 signal term_p0_g0_rp_rg0
[Series Pin Mapping] pin_2 model_name
1 2 series_r0_c
```

**Auto-generation for
IBIS Terminator / Series
models**

```
[Model] term_p0_g0_rp_rg0
Model_type Terminator
| variable typ min max
C_comp 0 NA NA
[Pullup Reference] 0 NA NA
[Pulldown Reference] 0 NA NA
[POWER Clamp Reference] 0 NA NA
[GND Clamp Reference] 0 NA NA
| variable typ min max
[Rgnd] 0 NA NA
```

```
[Model] series_r100K_c
Model_type Series
| variable typ min max
C_comp 0 NA NA
[Pullup Reference] 0 NA NA
[Pulldown Reference] 0 NA NA
[POWER Clamp Reference] 0 NA NA
[GND Clamp Reference] 0 NA NA
```

```
| variable typ min max
[R Series] 100K NA NA
```

Auto-Mapping Capability for Terminator Mapping

Device Model Mapping

R7	r7.ibs	RESISTOR_100K
R8	r8.ibs	RESISTOR_100K
R9	r9.ibs	"RESISTOR_7.5"
R10	r10.ibs	RESISTOR_0603_22
R11	r11.ibs	RESISTOR_0603_0
R12	r12.ibs	"RESISTOR_7.5"
RN1	rn1.ibs	RPACK_0603_22
RN2	rn2.ibs	RPACK_0603_22

IBIS File Name .ibs IBIS Comp Name

Terminator Setting

Resistance: Ohm Capacitance: Farad

Terminator

Automation Summary

```
R1 : RESISTOR_0603_22 -> 2PIN_R22
R2 : RESISTOR_0603_0 -> 2PIN_2GR0
R3 : RESISTOR_7.5 -> 2PIN_R7.5
R4 : RESISTOR_7.5 -> 2PIN_R7.5
R5 : RESISTOR_7.5 -> 2PIN_R7.5
R6 : RESISTOR_0603_22 -> 2PIN_R22
R7 : RESISTOR_100K -> 2PIN_1P2.5R100k
R8 : RESISTOR_100K -> 2PIN_2GR100k
R9 : RESISTOR_7.5 -> 2PIN_R7.5
R10 : RESISTOR_0603_22 -> 2PIN_R22
R11 : RESISTOR_0603_0 -> 2PIN_1GR0
R12 : RESISTOR_7.5 -> 2PIN_R7.5
RN1 : RPACK_0603_22 -> 8PI_R22
RN2 : RPACK_0603_22 -> 8PI_R22
RN3 : 2POS_RPACK_CRA0805_22_5_-> No Change
RN4 : RPACK_0603_22 -> 8PI_R22
RN5 : 2POS_RPACK_CRA0805_22_5_-> No Change
RN6 : RPACK_0603_22 -> 8PI_R22
```

Report

EBD Contents

Include DML Net Information **Preference**

Terminator Setting Automation

Resistor Prefix :

Capacitor Prefix :

Delimiter :

Usage : <Prefix><Delimiter>...<Delimiter><Value>

Prefix separator : ; semicolon

Model Mapping

R8	terminators.ibs	2PIN_2GR100k
R9	terminators.ibs	2PIN_R7.5
R10	terminators.ibs	2PIN_R22
R11	terminators.ibs	2PIN_1GR0
R12	terminators.ibs	2PIN_R7.5
RN1	terminators.ibs	8PI_R22
RN2	terminators.ibs	8PI_R22
RN3	rn3.ibs	2POS_RPACK_CRA0805_22_5_

Easy Terminator Work Wizard

- Detect Net connections
- Handles Isolated and Bussed type resistor packs
- Automatic embedding solutions for extended nets

Package Pin Connection (4 Pin)

Name: 4PIN_ISOLATED_

Net < > RefDes . Pin Name	Pair Pin
DQ7 < > RN3 . 1	4
DQ3 < > RN3 . 2	3
DQ3A < > RN3 . 3	2
DQ7A < > RN3 . 4	1

Bussed

Apply Cancel

Terminator Setting

Terminator

Resistance: 22 Ohm

Capacitance: Farad

Pin Connections

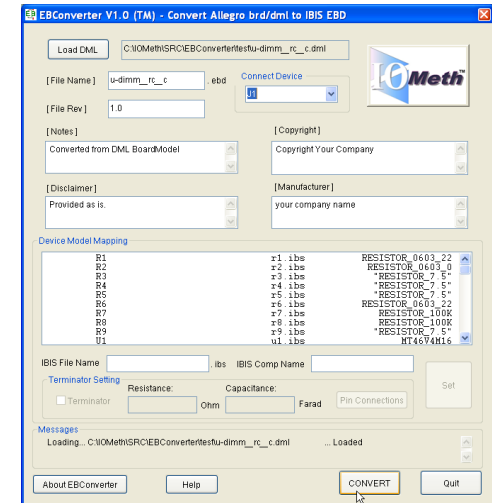
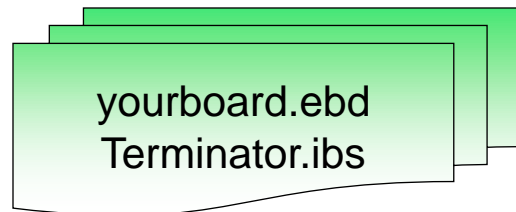
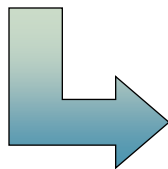
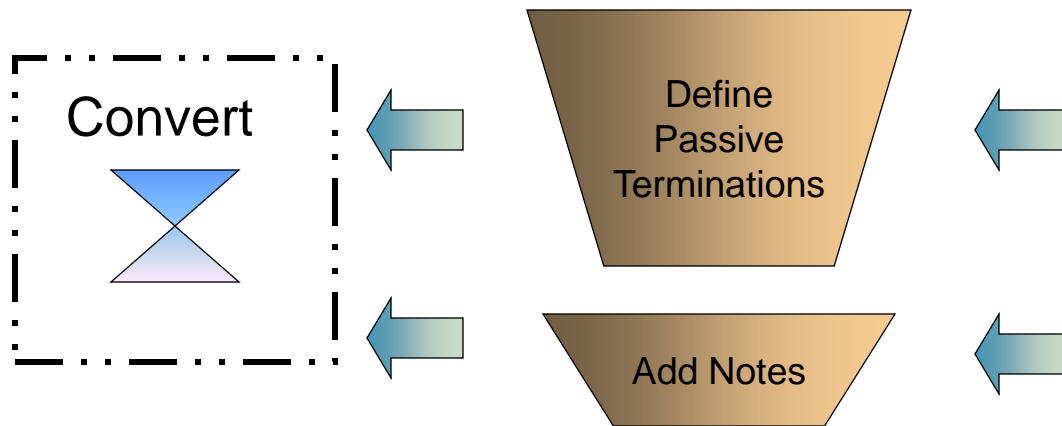
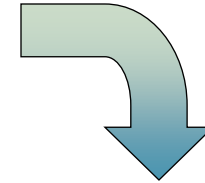
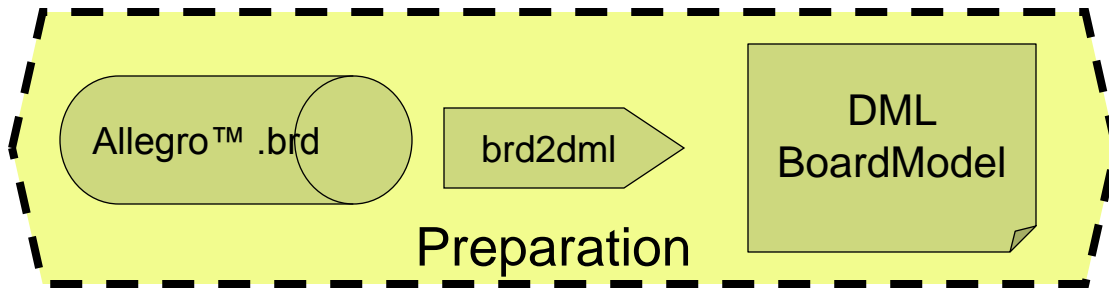
Informational comments/notes

```
|  
[Number Of Pins] 184  
|  
[Pin List] signal_name  
| J1.1  
1 POWER  
| J1.2  
2 DQ0  
| J1.3  
3 GND  
| J1.4  
4 DQ1  
| J1.5  
5 DQS0  
| J1.6  
6 DQ2  
| J1.7  
7 POWER  
| J1.8
```

```
[Path Description] DQ0  
| J1.2  
Pin 2  
| R@@X2130Yn370L1_@@J1.2  
| ignored for Spice simulators  
|Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/  
| XNTL_XSTLX2350Y970L1X2130Yn370L1  
Len=0.00382234 L=3.6466e-007 C=8.8655e-011 R=4.5129e+000/  
| R@@X2350Y970L1_@@RN1.1  
| ignored for Spice simulators  
|Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/  
| RN1.1 -> RN1.8 R=22  
Len=0 R=22/  
| Net: DQ0A  
| R@@X2350Y1370L1_@@RN1.8  
| ignored for Spice simulators  
|Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/  
| XNTL_XSTLX2350Y1370L1X4040Y5321L1  
Len=0.0145933 L=3.6466e-007 C=8.8655e-011 R=4.5129e+000/  
| R@@X4040Y5321L1_@@U1.54  
| ignored for Spice simulators  
|Len=0 L=0.0000e+000 C=0.0000e+000 R=1.0000e-006/  
Node U1.54
```

**Keep the information as the original board
Remain the segment info in EBD for easy verification**

Process Flow



Load in EBC

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- Convert your Allegro brd / dml to IBIS EBD model

Do It Quick!

Done It Right!