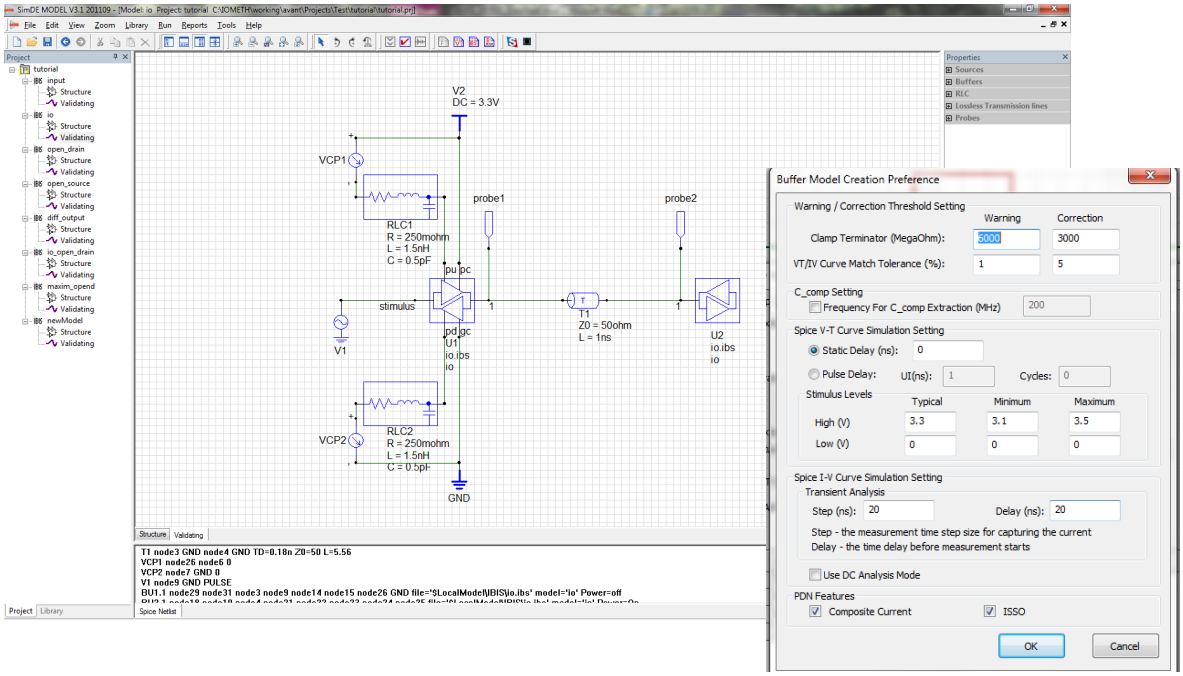
SimDE™ MODEL

The environment for Signal Integrity model generation and validation



- Automated IBIS Model Generation for
  - All types of IBIS buffer
  - True differential pair buffer using traditional IBIS buffers
  - IBIS 5.0 PDN models
- Automated SPICE macromodel generation with embedded Fitting functionality
  - Pre-emphasis
  - SSO/SSN driver and

SIMDE™ MODEL Overview

Simulation is more and more important for High-Speed system design. It can help you optimize your design performance, reduce your design cycle, lower your prototype cost and accelerate your design to market. Electrical I/O modeling is the starting point for your advanced chip and system simulations. It enables faster and more accurate simulations.

SIMDE™ Modeling provides a graphical model development and validation environment. It gives direct methods for model developments and validations. It focuses on automated SI model extraction, generation and validation processes.

Create accurate models with performance.

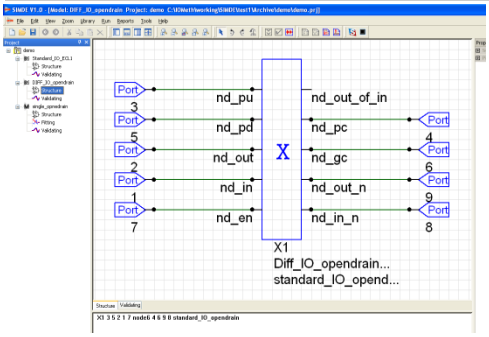
IBIS Model Generation and Validation

SimDE™ MODEL provides an automated IBIS buffer model extraction, generation and validation processes. It includes a graphical interface for mapping the SPICE buffer nodes as well as using the schematic type editing mode for other nodes settings. It automatically runs Synopsys HSpice to extract the buffer's behavior from the Spice buffer. There is no need for manual editing during the process.

SimDE™ MODEL has a seamless validation process for IBIS buffer model generation. It remembers all the settings for the Spice model when generating the IBIS buffer and uses them for your IBIS model validation on your own topologies. It also provides a detailed DPI (Differential Peak Index) and DAI (Differential Average Index) and reports any differences between the Spice and IBIS buffer simulations. A waveform clearly depicts the quality of the results.

SimDE™ MODEL contains:

- Automatic Spice buffer node mapping capability
- Graphical node setting capability
- Automatic Spice to IBIS buffer extraction process
- Auto Die-Capacitance extraction option for both driving and receiving mode.
- Capable for All IBIS Input / Output / IO model types and differential buffers (Pseudo, half and true differential pair) extractions with manual common-mode voltage setting option
- Easy setup for Typical / Minimum / Maximum corner extractions
- Supports IBIS 5.0 PDN [Composite Current] and [ISSO_*] extractions
- Supports HSpice, Spectre, Eldo, MSIM and TISpice3 integrations *
- Extraction using existing data for IBIS and IBIS differential models
- Build-in IBIS standard buffer test fixtures
- IBIS buffer model validation sheet with freedom of topology settings
- Detail validation reports with Differential Peak Index (DPI) and Differential Average Index (DAI)
- IBIS buffer curves visual inspection and report for On-die termination, non-monotonic and load-line crossing verification. (SimDE™ MODEL IBIS Application Module)
- IBIS file generation wizard with [Model Selector] builder
- Extraction simulation ONLY capabilities to be used for simulator queue script applications for both GUI and Batch-mode operations
- Supports true-differential current-mode IBIS buffer extractions
- Batch-mode operations for large number IBIS buffer generations in one project
- IBIS VT/IT curve initial delay trim capabilities
- IBIS VT/IT curve total length control
- IBIS VT/IT curve maximum point number control
- Stimulus Rising/Falling edge control for IBIS VT/IT curve extraction



Spice Macromodel Generation, Fitting and Validation

SimDE™ MODEL provides an integrated flow for Spice Macromodel Generation, Fitting and Validation. It allows a user to start from scratch or start from the base elements, using our integrated standard library elements or elements you made as black-boxes. Its hierarchy structure will give the user a clean graphical structural view from the different levels.

The Fitting process allows the user to load the Golden waveform for the macromodel optimization process. It can swing many parameters and find the best settings for the case that fits the Golden source the best.

The validation process takes place in an easy-to-use environment for verifying the macromodel that you just built for a specific load validation. You may also import 3rd party models for validation.

Product Configurations (Available for Windows and Linux OS platforms)

Features\Tiers		LEGACY	ADVANCE	EXPERT
IBIS Generation	IBIS Single-end	X	X	X
	IBIS Diffpair	X	X	X
	IBIS PDN		X	X
IBIS Validation	IBIS Single-end	X	X	X
	IBIS Diffpair	X	X	X
	IBIS PDN		X	X
Spice Macromodel	Schematic Builder			X
	Fitting			X
	Validation			X
Utility Tools	WAVEFORM 2D	X	X	X
	WAVEFORM 3D		X	X
	IBIS VALIDATOR	X	X	X
	IBISGEN BATCH			X

Product Support / Maintenance

This is a yearly fee-based service including technical Q&A, bug fixing service packs and product enhancement updates. Product technical training is available for an additional cost to customers on maintenance.

* Spectre, TiSpice3 integrations are only available for Linux OS.