
SimDETM *MODEL*

Modeling your device with performance and accuracy

V4.2 - Release 201309



What's New in V4.2 201309

- Supports IBIS VT/IT initial delay trim requirement
- Enabled to specify stimulus Rising/Falling edges for VT curve extractions
- Enabled to specify IBIS VT/IT curve total length control
- Allowed user to specify the maximum VT/IT point numbers for file size reduction

SimDE™ MODEL

- **The first complete IBIS model development and validation tool**
 - Support all IBIS buffer type extraction / generation
 - Automated differential IBIS model (True, Pseudo and Half) extraction / generation
 - Integrated IBIS model validation for single-end and differential-pair IBIS buffers
 - Support IBIS 5.0 PDN feature extractions
- **The industry first Spice Macromodel development tool with Fitting and Validating functionalities**
 - Support advance digital buffer model development
 - Automated Fitting and Validating functionalities with golden waveforms
 - Support analog model development

IBIS VT/IT initial delay trim and curve length control

C_Comp Setting

☐ Frequency For C_comp Extraction (MHz) 100

Spice V-T Curve Simulation Setting

☒ Static Delay(ns): 2 IBIS VT-IT Length(ns) 10.000

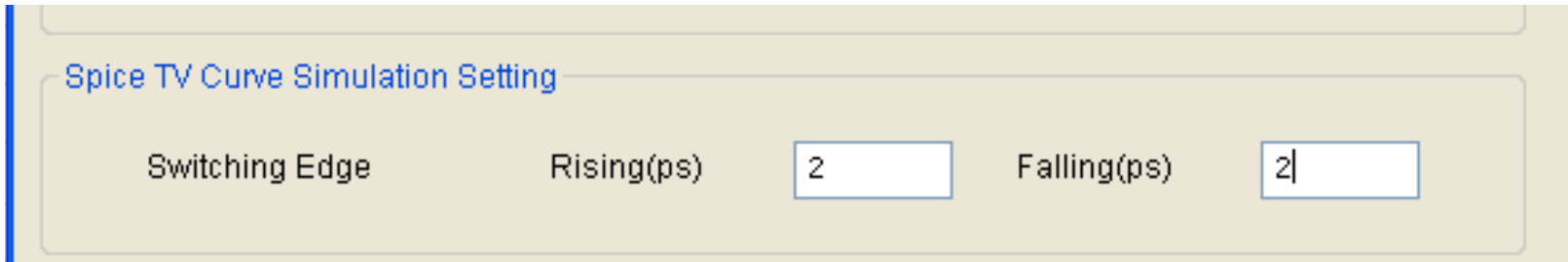
☐ Pulse Delay: UI(ns): 10 Cycle: 2

| | Typical | Minimum | Maximum |
|---------------------|---------|---------|---------|
| Init-Delay Trim(ns) | 0.2 | 0.2 | 0.08 |
| Stimulus_High(V) | 3.3 | 3.1 | 3.5 |
| Stimulus_Low(V) | 0 | 0 | 0 |
| Max. VT Points | 400 | | 300 |
| Time Step(ps) | 25 | | 12.080 |

Spice I-V Curve Simulation Setting

Proper Initial delay trim and curve length control will help for overclocking issue in IBIS simulations

Stimulus Rising / Falling edge control for IBIS VT extraction



The image shows a software interface for configuring simulation settings. It features a title bar at the top, followed by a section header "Spice TV Curve Simulation Setting". Below this, there is a row of controls. On the left is a label "Switching Edge". To its right are two input fields. The first is labeled "Rising(ps)" and contains the value "2". The second is labeled "Falling(ps)" and contains the value "2".

| Switching Edge | Rising(ps) | Falling(ps) |
|----------------|------------|-------------|
| | 2 | 2 |

This feature enables the total control for VT extraction stimulus configurations. It will allow to generate more accurate models for new advanced buffers

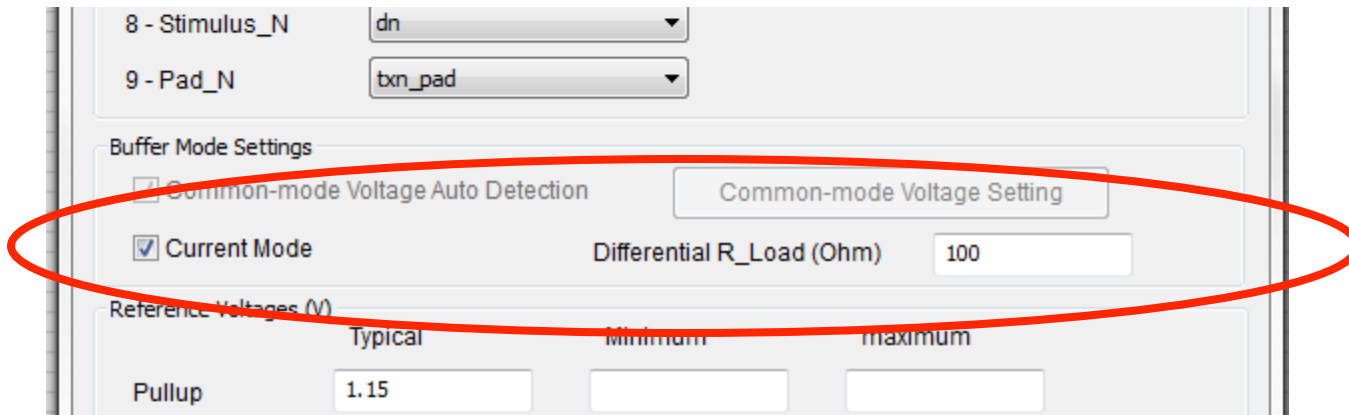
IBIS VT/IT Maximum Point Number Control

The most of times, VT/IT curves will only need few hundred points for keeping the accuracy of the models. This maximum number control will allow to minimize the file size significantly.

The screenshot shows the 'Spice V-T Curve Simulation Setting' section of a software interface. A red oval highlights the 'Max. VT Points' and 'Max. IT Points' fields, which are set to 400 and 300 respectively. Other visible settings include:

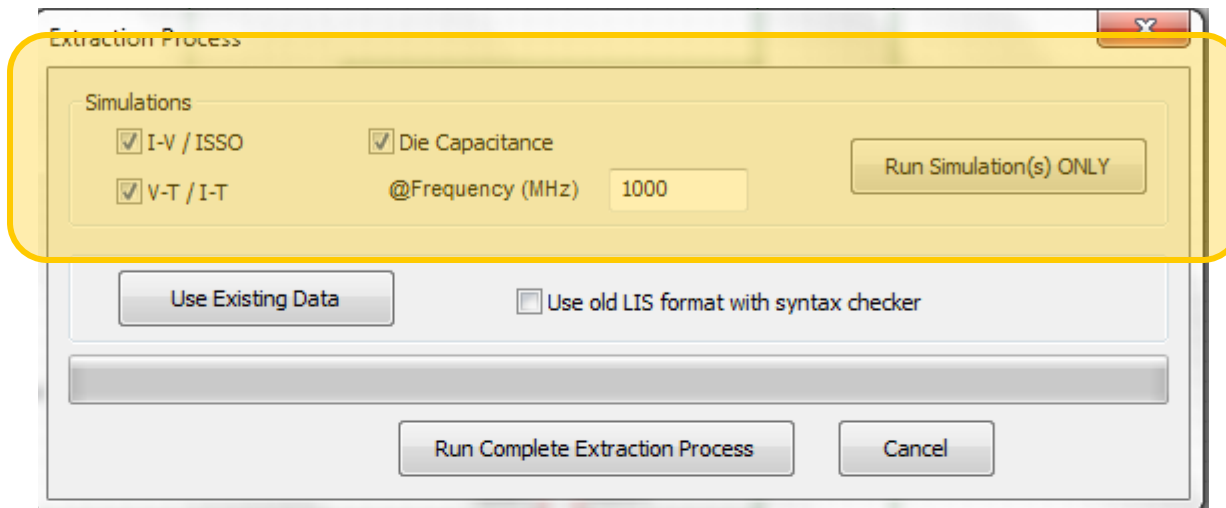
- C_Comp Setting:** ☐ Frequency For C_comp Extraction (MHz) set to 100.
- Spice V-T Curve Simulation Setting:**
 - ☒ Static Delay(ns): 2, IBIS VT-IT Length(ns): 10,000
 - ☐ Pulse Delay: UI(ns): 10, Cycle: 2
 - Init-Delay Trim(ns): Typical (0.2), Minimum (0.2), Maximum (0.08)
 - Stimulus_High(V): 3.3, 3.1, 3.5
 - Stimulus_Low(V): 0, 0, 0
 - Max. VT Points: 400, Max. IT Points: 300
 - Time Step(ps): 25, Time Stop(ns): 12,080
- Spice I-V Curve Simulation Setting:** (partially visible)

Current-Mode True-differential pair Support



Out of ordinary IBIS extraction methods with enhanced Weighted Best Point Reduction algorithm for accurate current-mode true-differential IBIS buffer model extractions

Selectable Extraction Simulation ONLY options for time consuming long simulations



Using script for simulation queue. Simulate first, extraction process using existing data later

Enhanced batch-mode operation for large number buffer generations in one project

```
C:\IOMETH>bibisgen

SimDE MODEL batch command program - IBISGEN
Copyright 2006-2012 IO Methodology Inc. All rights reserved.

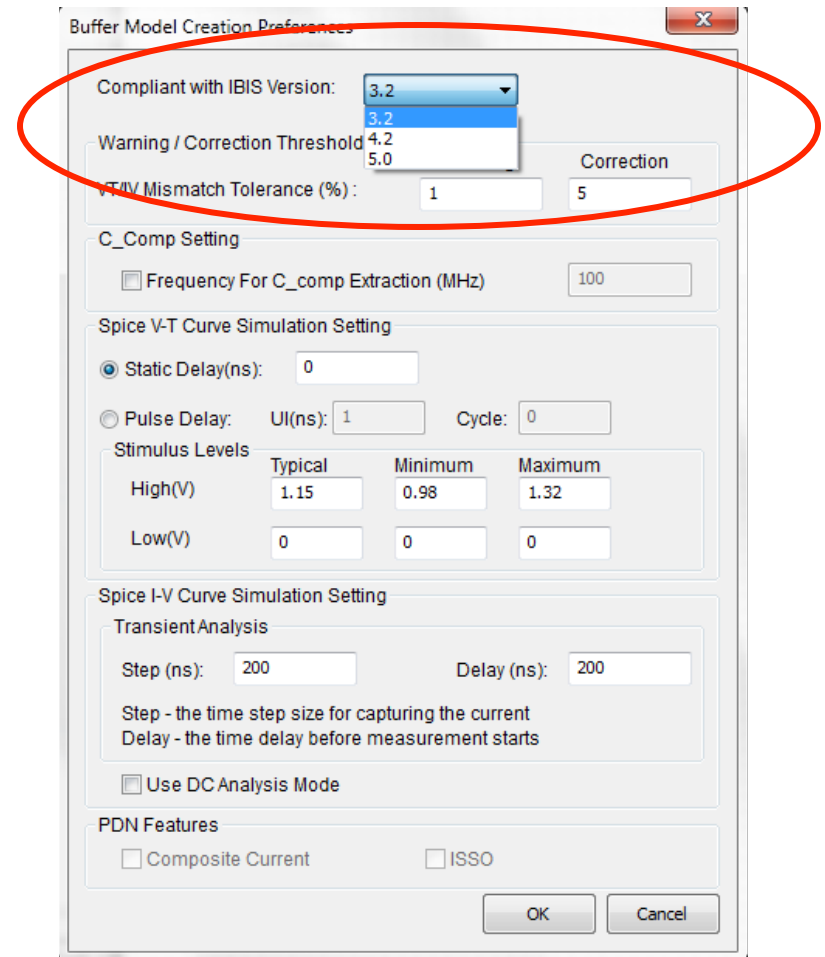
Missing SimDE MODEL Project(.prj) file

Help:
Usage: bIBISGen (project file .prj) <option>
Options: (case sensitive)
-SimOnly: Simulations Only
-CapSimFreq: DieCap Extraction Frequency in MHz (need to be used with -SimOnly option)
-h or -Help: Help Contents
Examples: bIBISGen test.prj
          bIBISGen test.prj -SimOnly
          bIBISGen test.prj -SimOnly -CapSimFreq 2500

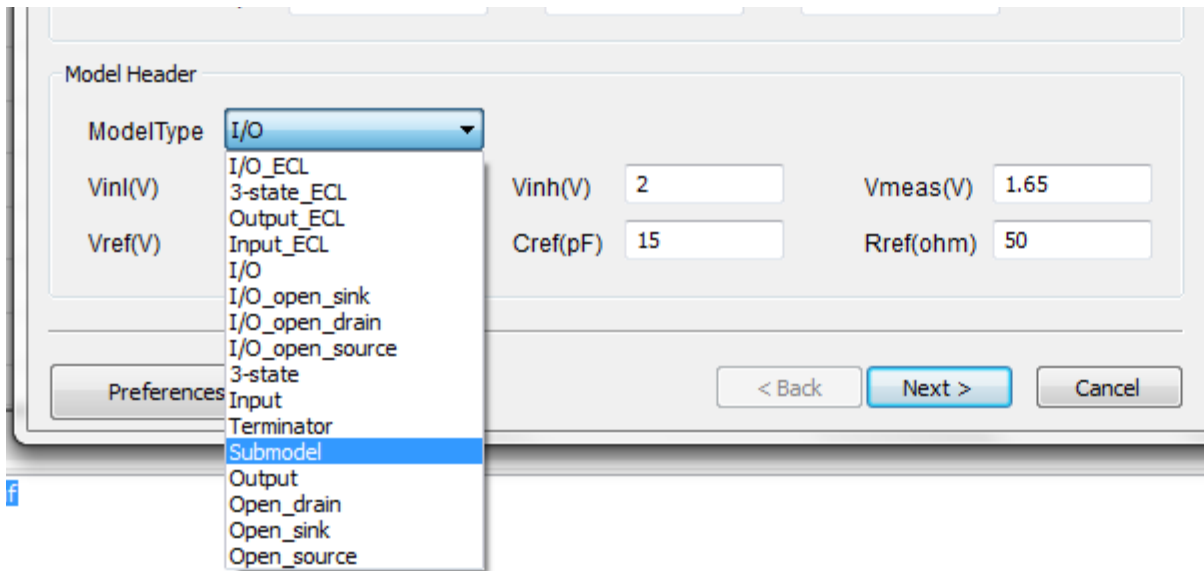
C:\IOMETH>_
```


Flexibility for IBIS version 3.2/4.2/5.0 buffer model generation to fit your customer needs

Choose the IBIS version your customer needs. SimDE™ will automatically generate version compatible IBIS buffers.



Supports SubModel (Dynamic Clamping) IBIS model type extractions



IBIS 5.0 PDN features with build-in test circuit

The screenshot displays the SimDE MODEL V3.1.1 201109 interface. The main window shows a circuit diagram with components including VCP1, VCP2, RLC1, RLC2, V1, V2, probe1, probe2, and T1. The circuit is connected to a stimulus source and a ground. The diagram includes labels for various nodes and components, such as "stimulus", "pd gc", "io.ibs", "io", "pu pc", "T1", "Z0 = 50ohm", "L = 1ns", "V2 DC = 3.3V", "probe1", "probe2", "VCP1", "RLC1", "R = 250mohm", "L = 1.5nH", "C = 0.5pF", "VCP2", "RLC2", "R = 250mohm", "L = 1.5nH", "C = 0.5pF", "V1", "GND".

The Buffer Model Creation Preference dialog box is open, showing various settings. The "Warning / Correction Threshold Setting" section includes "Clamp Terminator (MegaOhm): 5000" and "VT/IV Curve Match Tolerance (%): 1". The "C_comp Setting" section includes "Frequency For C_comp Extraction (MHz): 200". The "Spice V-T Curve Simulation Setting" section includes "Static Delay (ns): 0" and "Pulse Delay: UI(ns): 1 Cycles: 0". The "Stimulus Levels" table shows typical, minimum, and maximum values for High (V) and Low (V). The "Spice I-V Curve Simulation Setting" section includes "Transient Analysis" with "Step (ns): 20" and "Delay (ns): 20". The "Use DC Analysis Mode" checkbox is checked. The "PDN Features" section includes "Composite Current" and "ISSO" checkboxes, both of which are checked. The "OK" button is highlighted with a red circle.

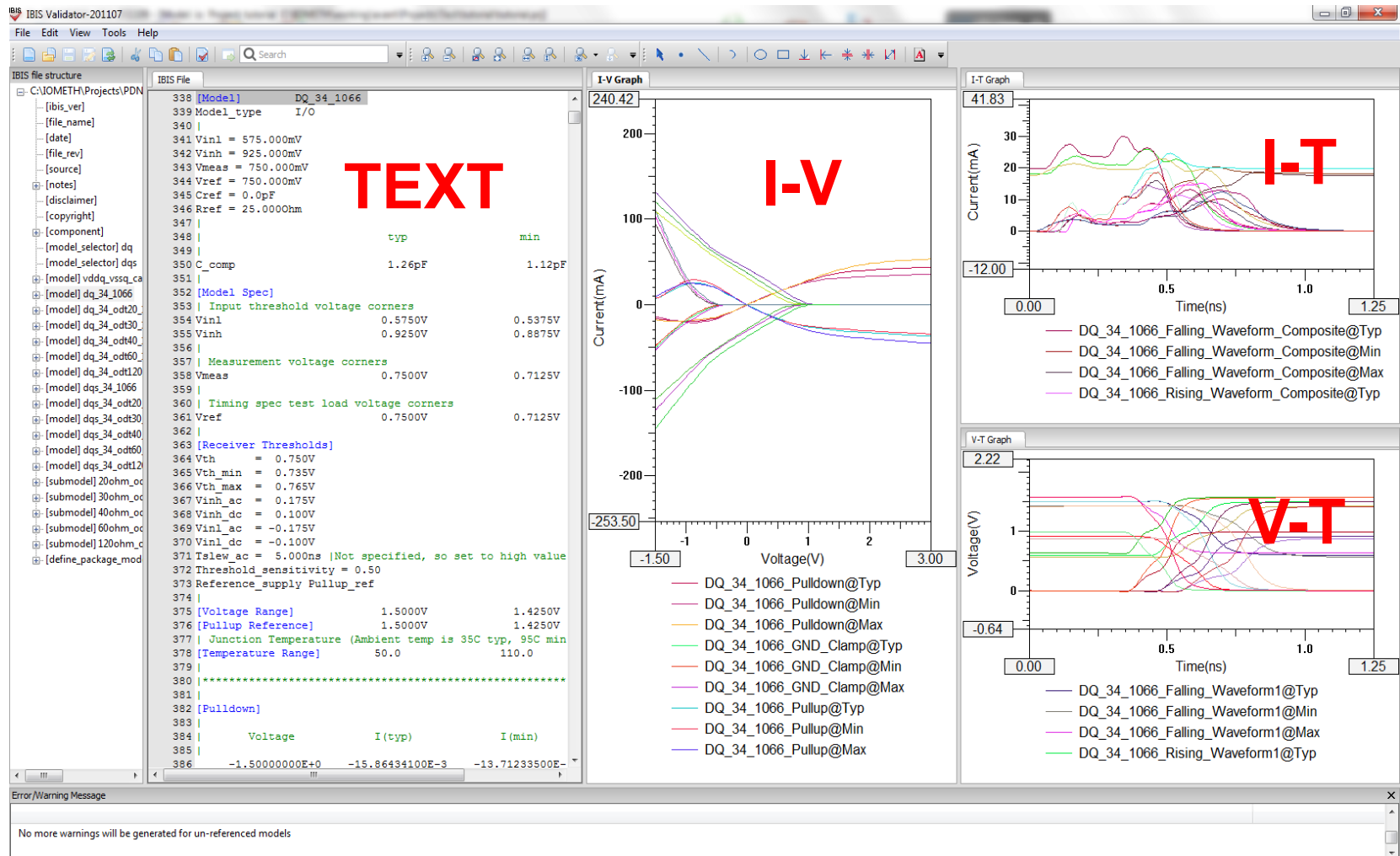
Project: tutorial
IBIS input
IBIS io
IBIS open_drain
IBIS open_source
IBIS diff_output
IBIS io_open_drain
IBIS io_maxim_opend
IBIS newModel

Structure Validating

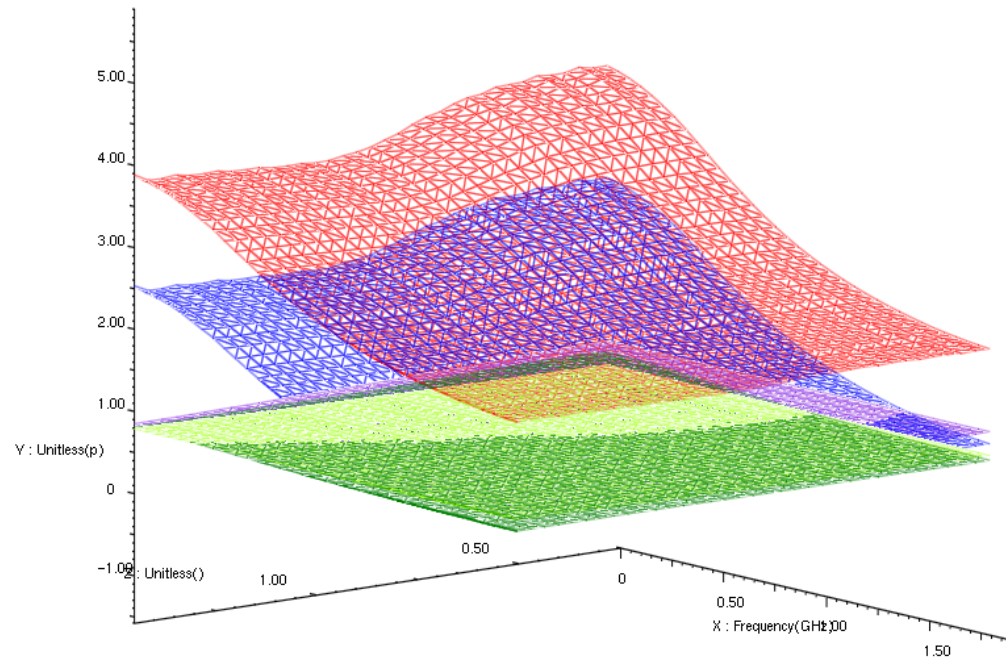
T1 node3 GND node4 GND TD=0.18n Z0=50 L=5.56
VCP1 node26 node6 0
VCP2 node7 GND 0
V1 node9 GND PULSE
BU1.1 node29 node31 node3 node9 node14 node15 node26 GND file="S:\LocalModel\IBIS\io.ibs" model="io" Power=off
BU2.1 node18 node4 node21 node22 node23 node24 node25 file="S:\LocalModel\IBIS\io.ibs" model="io" Power=on

Project Library
Spice Netlist
Ready

IBIS VALIDATOR



WAVEFORM 3D View



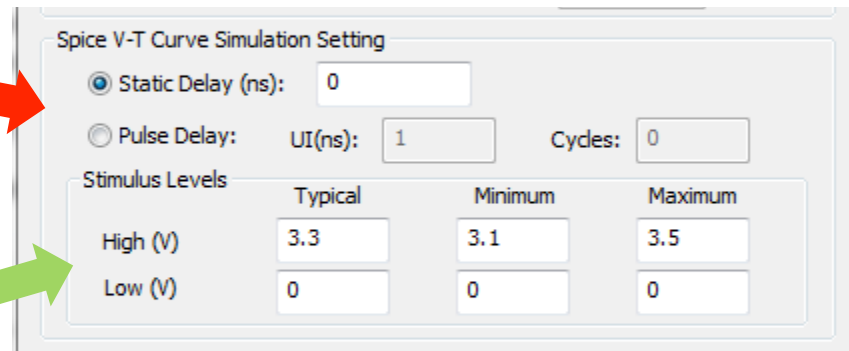
Flexible stimulus controls for IBIS model generations

■ Delays

- Static
- Pulse

■ Levels

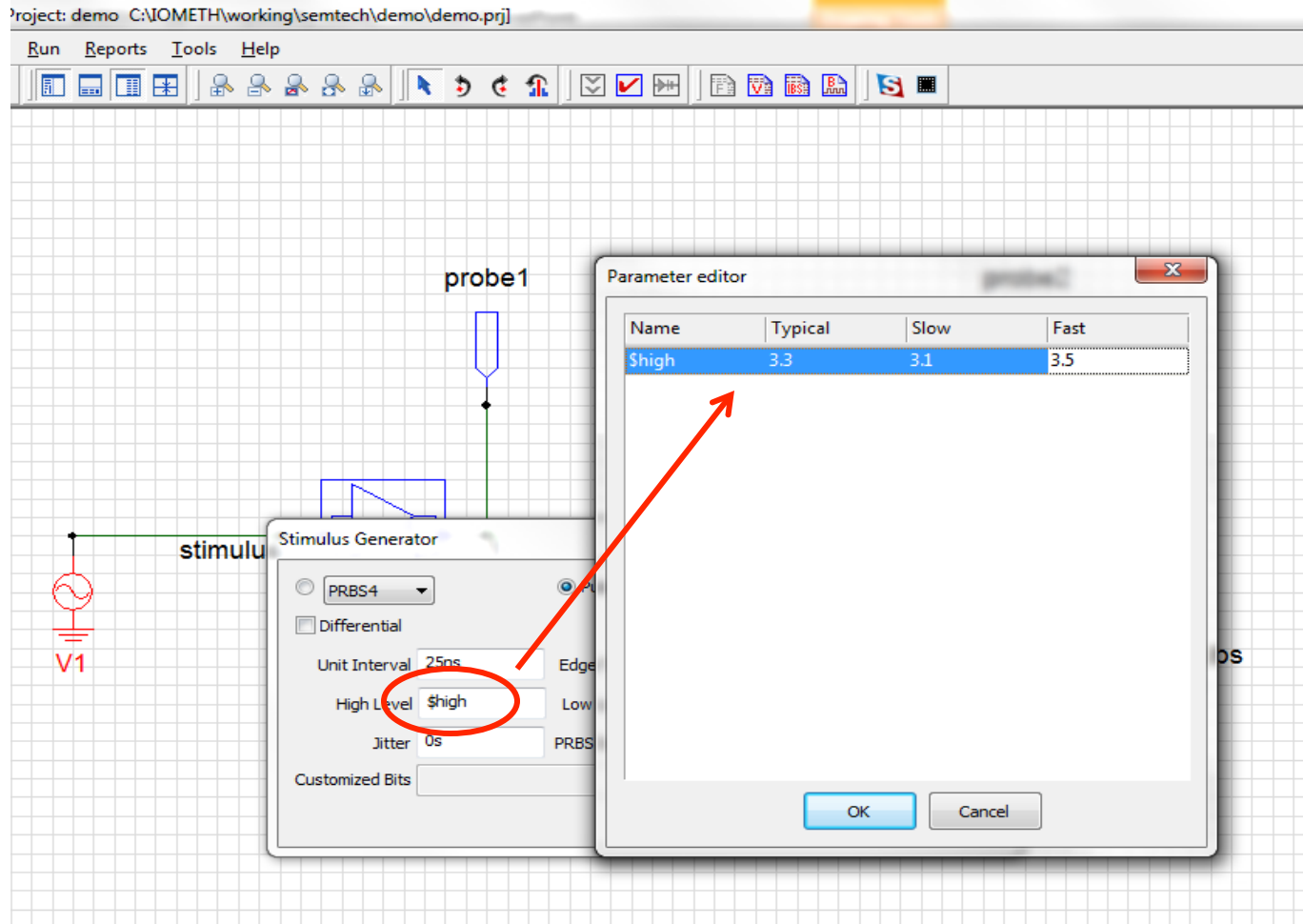
- High/Low
- Typ/Min/Max



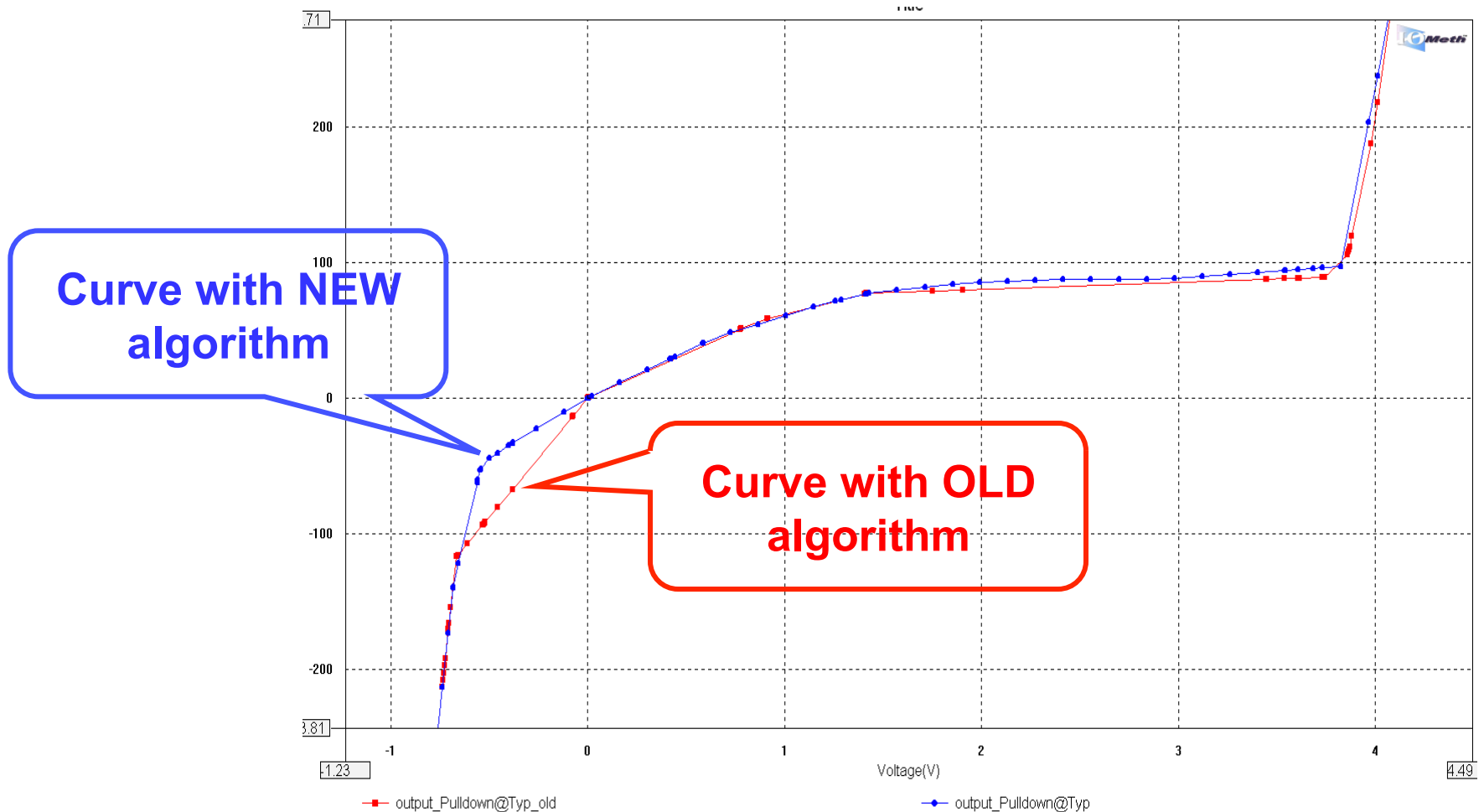
The image shows a 'Spice V-T Curve Simulation Setting' dialog box. It has two radio buttons: 'Static Delay (ns):' which is selected and has a value of '0', and 'Pulse Delay:' which is unselected and has sub-fields for 'UI(ns):' with a value of '1' and 'Cycles:' with a value of '0'. Below these is a 'Stimulus Levels' section containing a table with three columns: 'Typical', 'Minimum', and 'Maximum'. The table has two rows: 'High (V)' and 'Low (V)'. A red arrow points from the 'Static' bullet point to the 'Static Delay' radio button, and a green arrow points from the 'High/Low' bullet point to the 'Stimulus Levels' table.

| Stimulus Levels | Typical | Minimum | Maximum |
|-----------------|---------|---------|---------|
| High (V) | 3.3 | 3.1 | 3.5 |
| Low (V) | 0 | 0 | 0 |

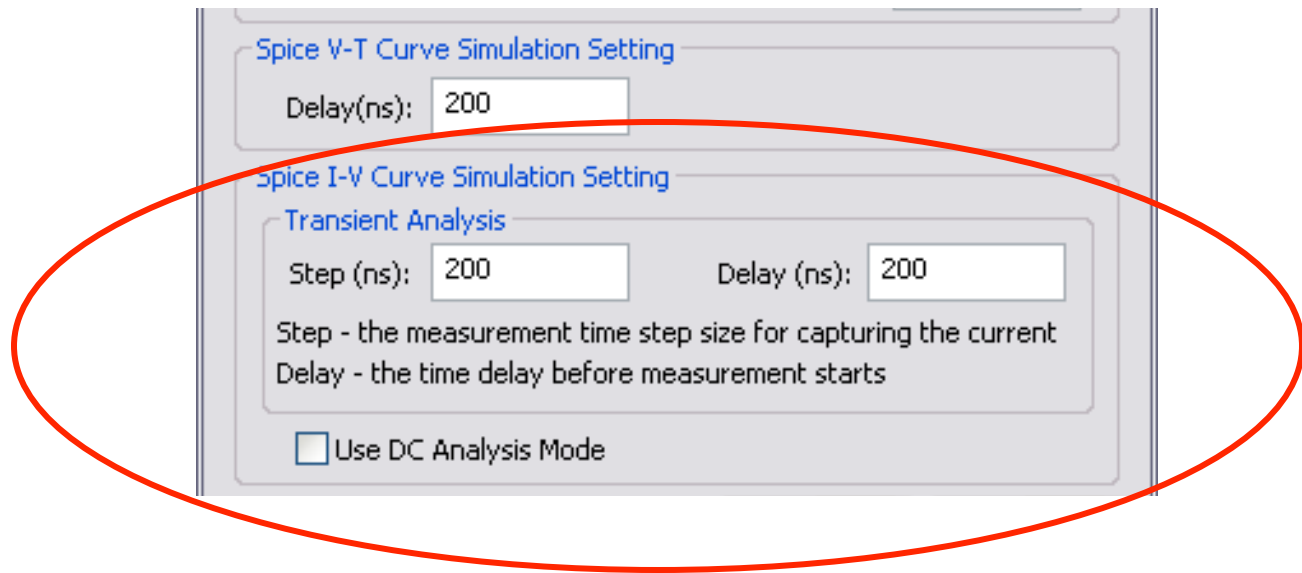
Stimulus level control for different corner IBIS validations



Advanced “weighted” Best-Point algorithm for I-V curve representations



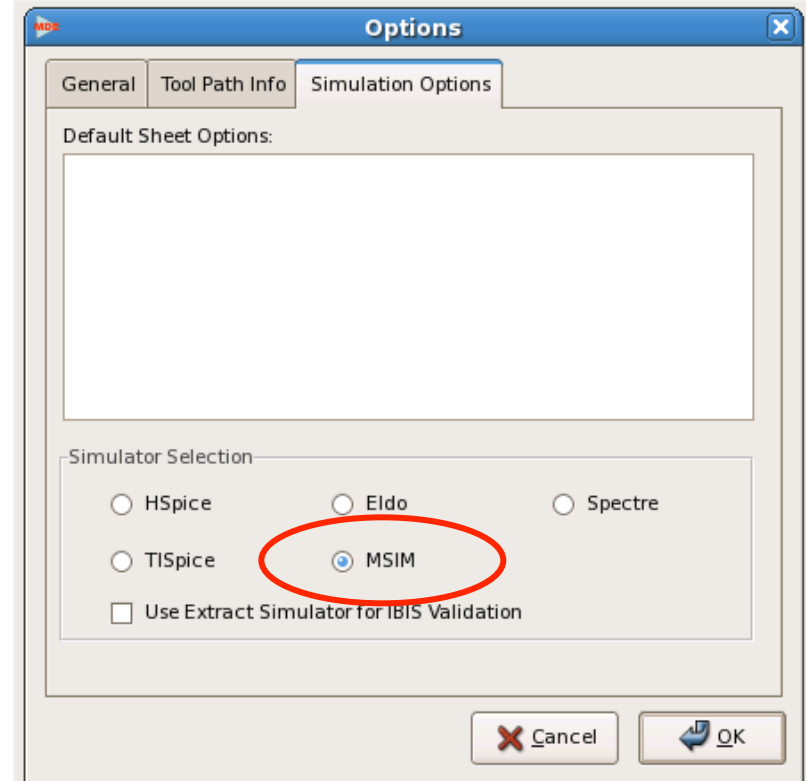
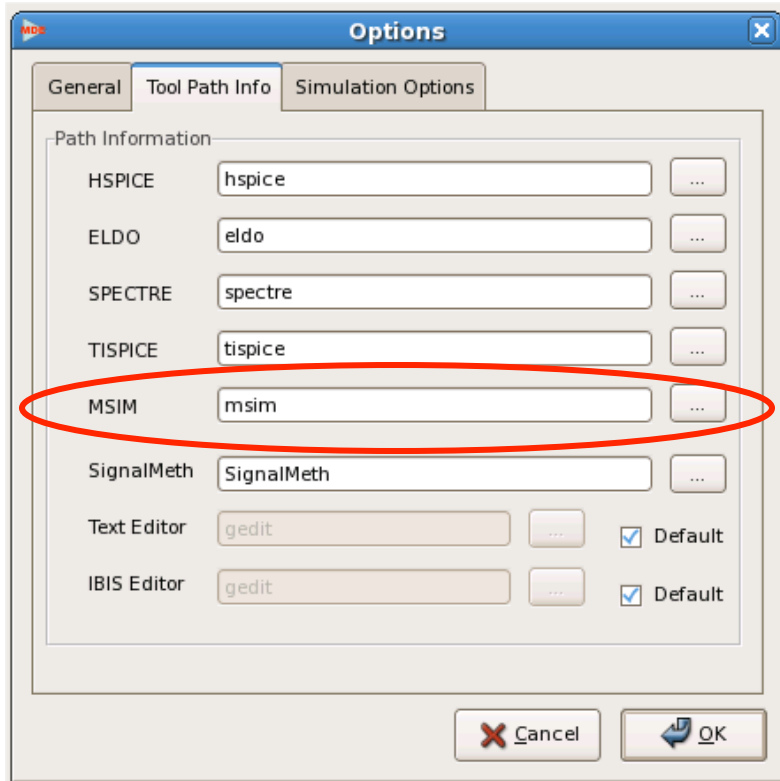
Both Transient and DC analysis modes available for I-V curve extractions



Insured to get the best result for I-V curve extractions

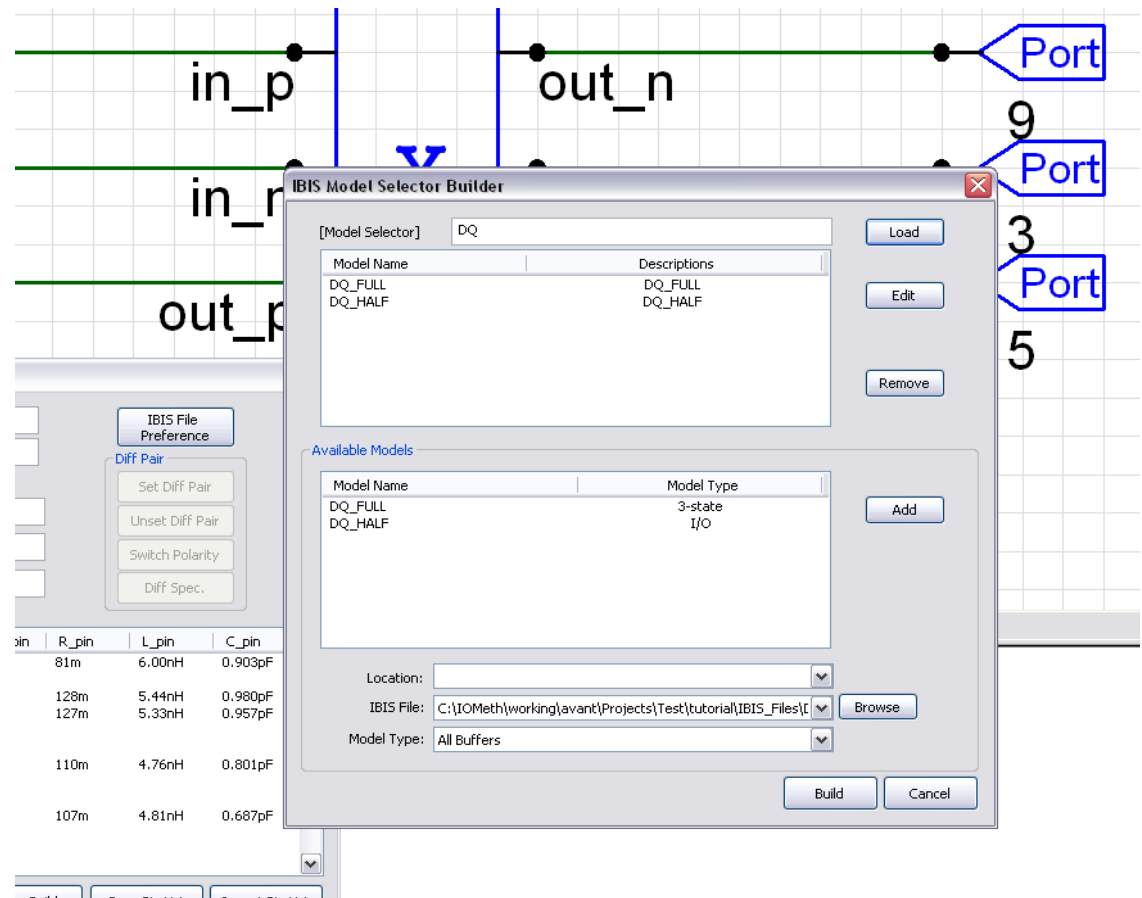
Spectre DC Analysis mode is not available in V2.2

Integrated MSIM simulator support for extraction and validation



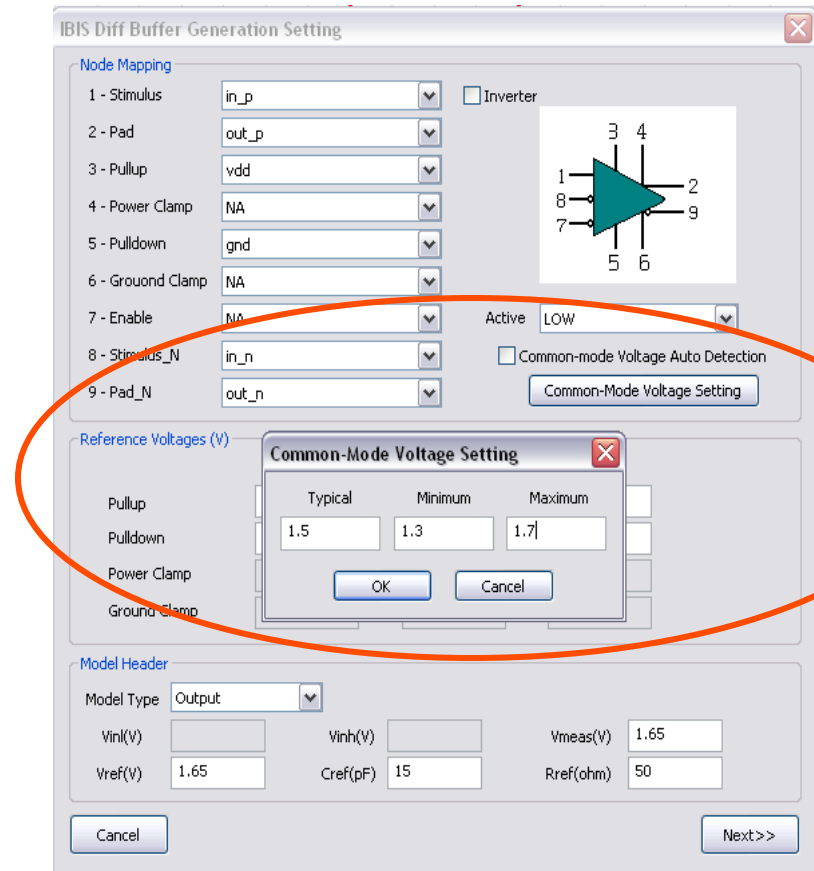
Model Selector Builder

- Build [Model Selector] from different IBIS files
- Load, Edit, Remove functionalities
- Can be added as a pin in IBIS file generation wizard



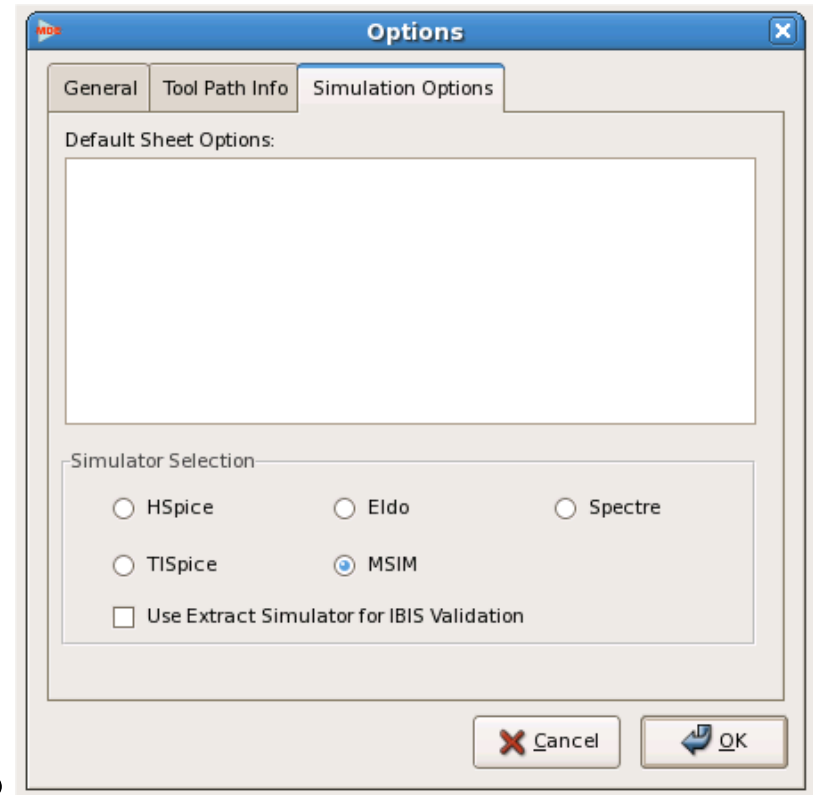
Manual Common-mode voltage setting option for differential pair IBIS extractions

- Manual common-mode voltage setting option
- Auto-detection still available
- Increase IBIS buffer model accuracy by setting precision common-mode voltages for each corner

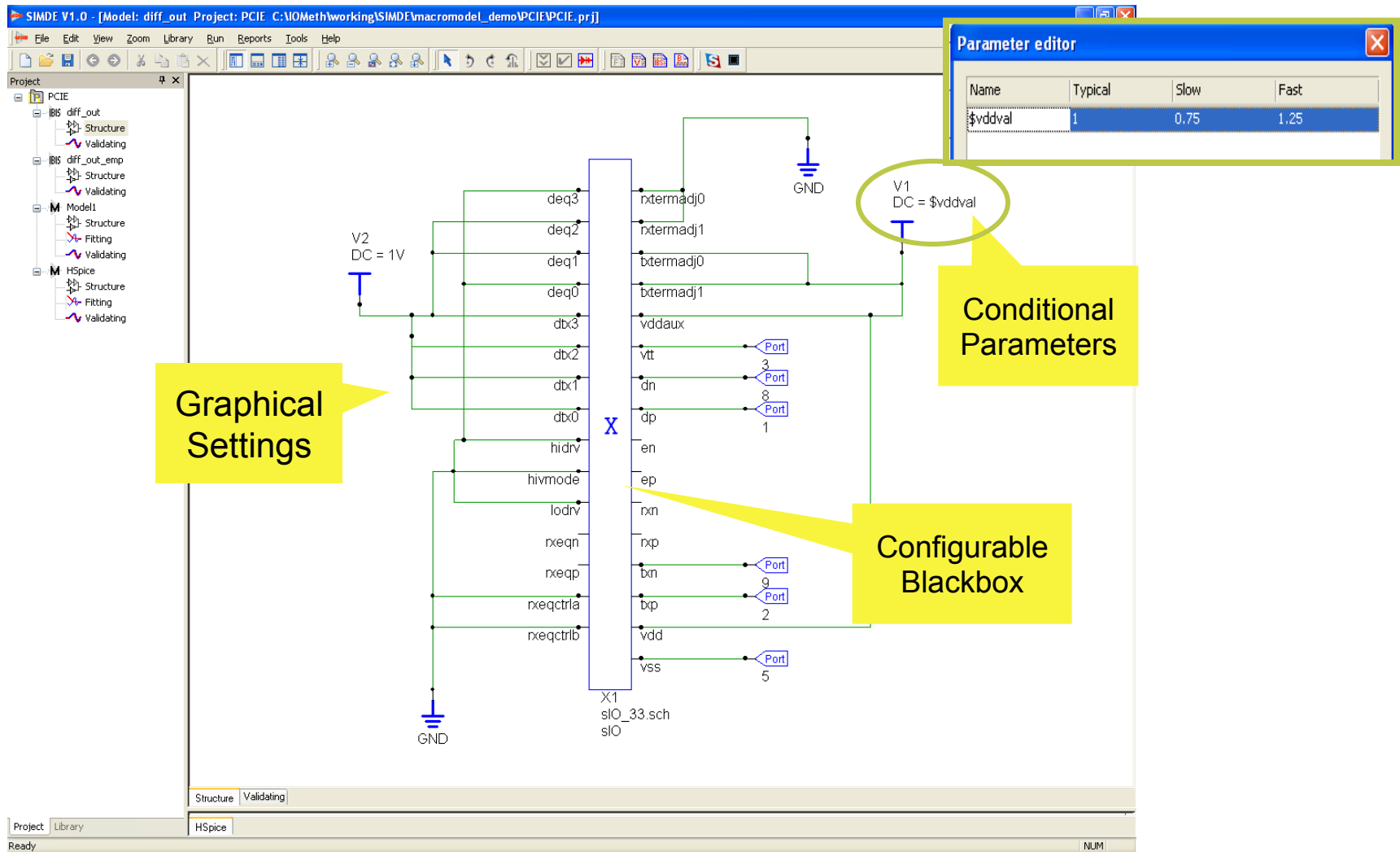


Multiple Simulator integrations

- Supports
 - Synopsys HSpice
 - Cadence Spectre
 - Mentor Eldo
 - Texas Instrument Spice3
 - Legend MSIM
- Seamless switching capability



IBIS Buffer Generation



IBIS Generation Setting Wizards

IBIS Diff Buffer Generation Setting

Node Mapping

1 - Stimulus: dp ☐ Inverter
2 - Pad: bxp
3 - Pullup: vtt
4 - Power Clamp: NA
5 - Pulldown: vss
6 - Ground Clamp: NA
7 - Enable: NA
8 - Stimulus_N: dn
9 - Pad_N: bxn

Active: LOW

Reference Voltages (V)

| | Typical | Minimum | Maximum |
|--------------|---------|---------|---------|
| Pullup | 1.5 | 1.1 | 1.9 |
| Pulldown | 0 | 0 | 0 |
| Power Clamp | 1.5 | 1.1 | 1.9 |
| Ground Clamp | 0 | 0 | 0 |

Model Header

Model Type: Output

Vin(V): Vinh(V): Vmeas(V): 0.75
Vref(V): 0.75 Cref(pF): 15 Rref(ohm): 50

Cancel Next>>

Node Mapping

C_comp Extraction

IBIS Buffer Parameter Setting

C_Comp (pF)

☒ Extract
Typical: Minimum: Maximum:

Temperature (Centigrade Degree)

Typical: 25 Minimum: 100 Maximum: 0

Test Fixture

R_fixture (ohm): 50 C_fixture(pF): 0 V_fixture Setting...

Spice VT Curve Simulation Setting

.TRAN Setting Time Step (ps): 25 Time Stop (ns): 15

LIB

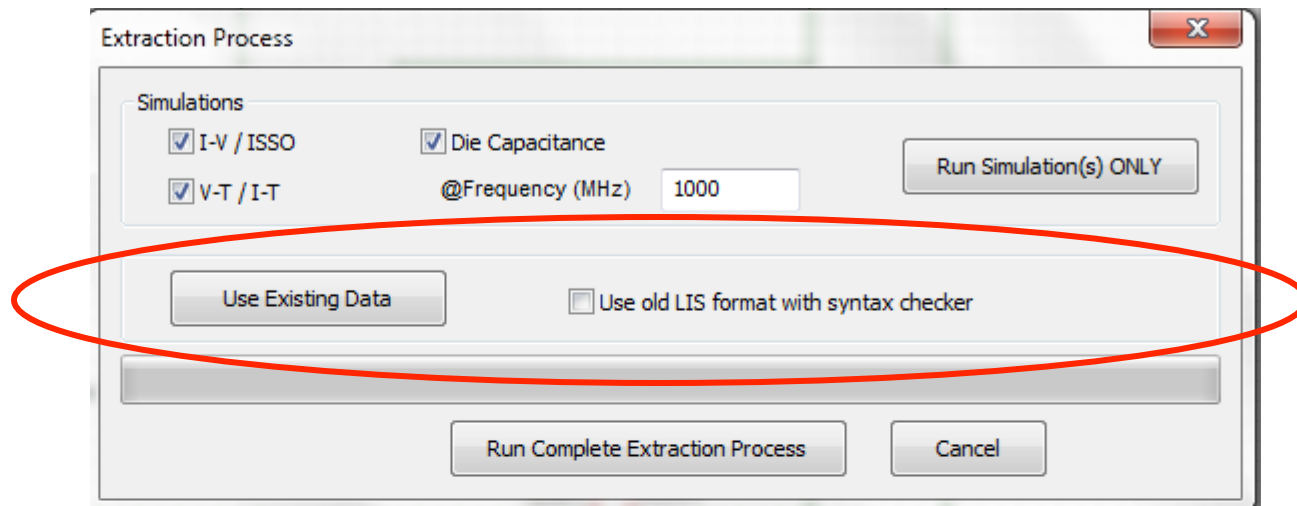
| Lib File | Lib | Typ | Slow | Fast |
|---------------------------------|---------|-------------------------------------|--------------------------|--------------------------|
| C:\IO METH\working\S... TT_g | TT_g | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| C:\IO METH\working\S... tt | tt | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| C:\IO METH\working\S... TT_33 | TT_33 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| C:\IO METH\working\S... TT_na33 | TT_na33 | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| C:\IO METH\working\S... DIO | DIO | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> |
| ... | | | | |

Cancel Preference << Previous OK

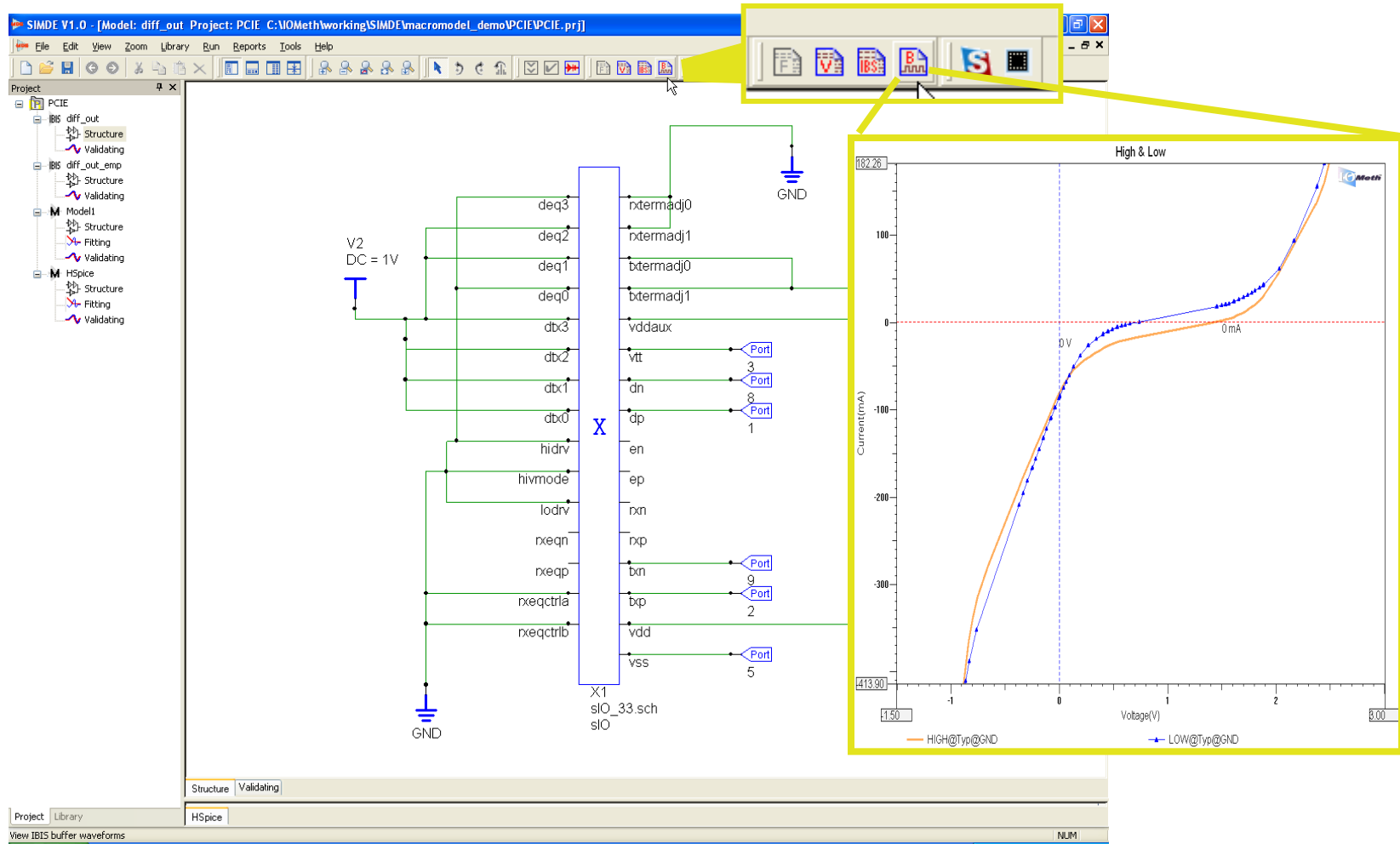
Node Mapping

Extraction with existing data

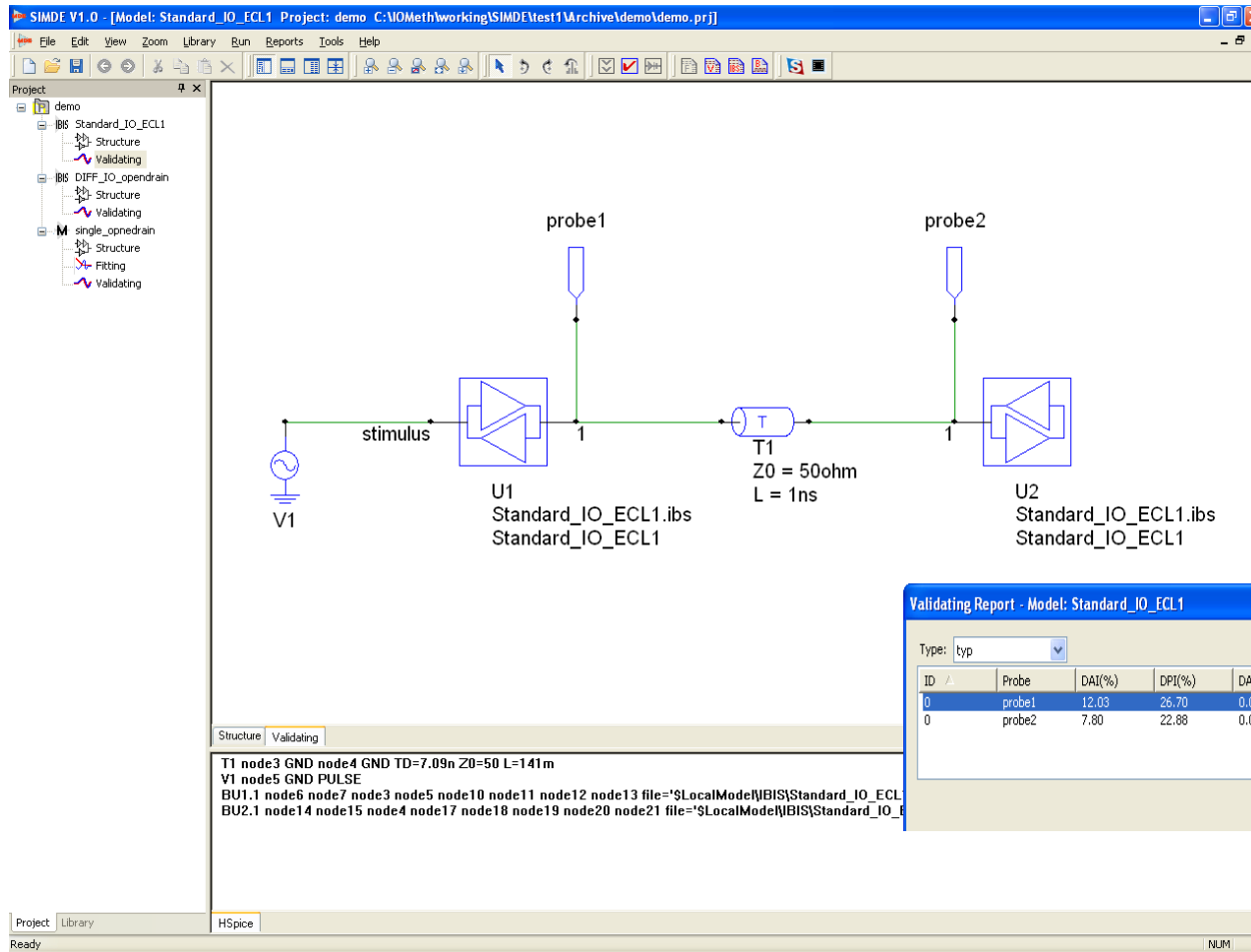
- Save simulation time
- Capable for other simulator and / or measurement output
- With syntax checker



Easy IBIS curve inspection



Build-in Test circuit and Flexible Topology Editor for Validations



Differential report

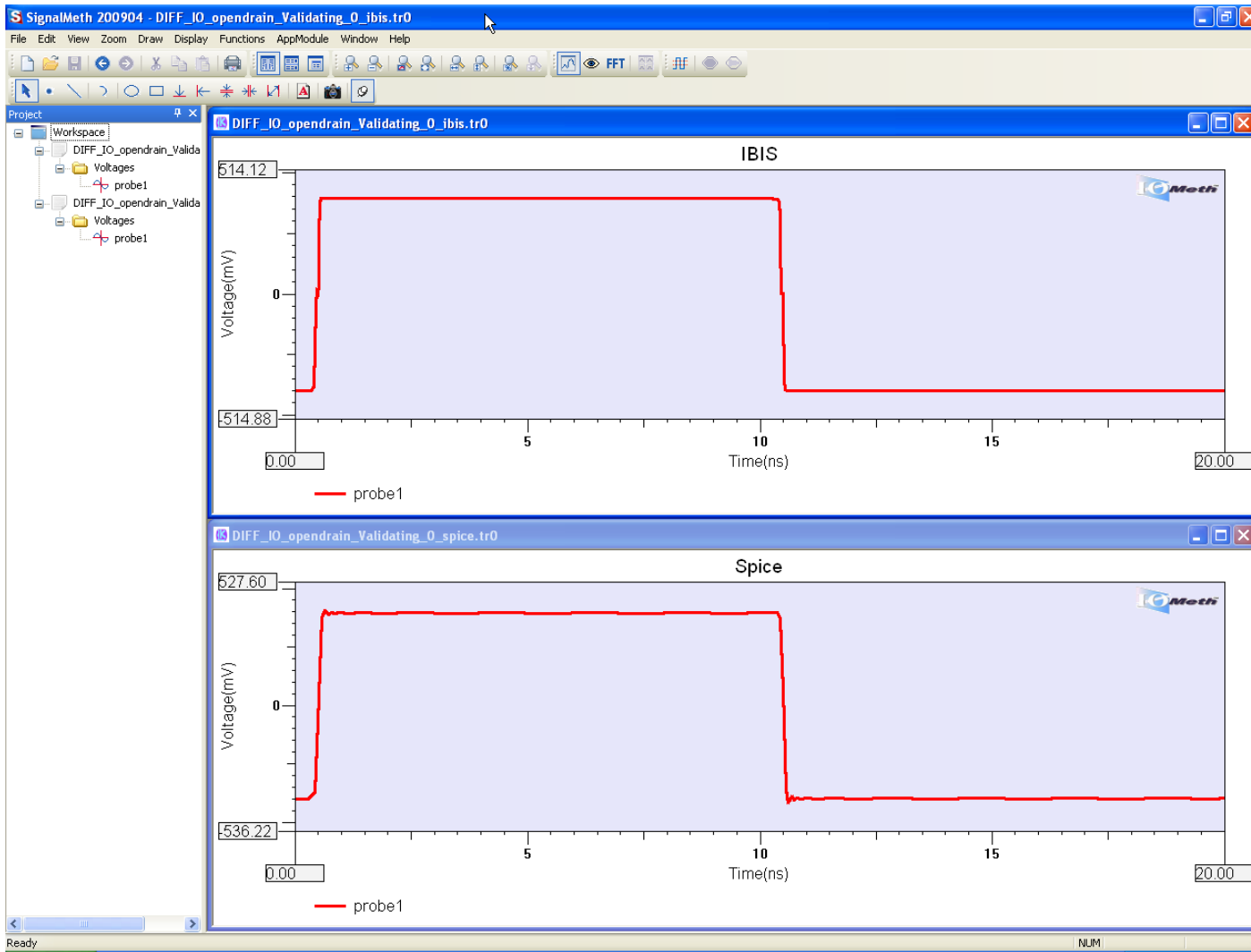
Validating Report - Model: Standard_IO_ECL1

Type: typ

| ID | Probe | DAI(%) | DPJ(%) | DA | DP |
|----|--------|--------|--------|------|------|
| 0 | probe1 | 12.03 | 26.70 | 0.09 | 0.19 |
| 0 | probe2 | 7.80 | 22.88 | 0.09 | 0.28 |

IBIS Sim Log Spice Sim Log View Waveform Close

Seamless Validation



Comprehensive IBIS File Builder

Creating IBIS Component

File Name: IBIS File Preference

[Component]:

[Package]

| Type | Min | Max |
|---------------------------------------|---------------------------------|---------------------------------|
| R_pkg <input type="text" value="0m"/> | <input type="text" value="0m"/> | <input type="text" value="0m"/> |
| L_pkg <input type="text" value="0n"/> | <input type="text" value="0n"/> | <input type="text" value="0n"/> |
| C_pkg <input type="text" value="0p"/> | <input type="text" value="0p"/> | <input type="text" value="0p"/> |

Diff Pair
Set Diff Pair
Unset Diff Pair
Switch Polarity
Diff Spec.

| [Pin] | Signal_Name | Model_Name | Model_Type | Diff_pin | R_pin | L_pin | C_pin |
|-------|-------------|------------|------------|----------|---------|-----------|-----------|
| 2 | Q0B | QOUT | Output_ECL | (+)1 | 0.45016 | 2.31200nH | 0.39282pF |
| 1 | Q0 | QOUT | Output_ECL | (-)2 | 0.41551 | 2.46728nH | 0.46661pF |

Edit Add Remove Save Pin List Import Pin List Generate Cancel Help

IBIS Component - Add Pin

[Pin]:

Signal Name: Assign

Signal Model:

☐ Power ☐ Ground ☒ Signal ☐ NC

Pin Parasitics
R_pin: L_pin: C_pin:

Signal Information
Location: Browse
Model File: Browse
IBIS Component:
Model Type:

| [Pin] | Signal_Name | Model_Name | Diff_pin | R_pin | L_pin | C_pin |
|-------|-------------|------------|----------|---------|-----------|-----------|
| 1 | Q0 | QOUT | | 0.41551 | 2.46728nH | 0.46661pF |
| 2 | Q0B | QOUT | | 0.45016 | 2.31200nH | 0.39282pF |
| 3 | Q1 | QOUT | | 0.45022 | 2.31675nH | 0.39342pF |
| 4 | Q1B | QOUT | | 0.41536 | 2.47060nH | 0.46538pF |
| 6 | DB | DIN_S | | 0.24315 | 1.88180nH | 0.44363pF |
| 7 | D | DIN_S | | 0.24302 | 1.86517nH | 0.44245pF |

OK Cancel

Macromodel Builder

SIMDE V1.0 - [Model: Model1 Project: PCIE C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\PCIE.prj]

File Edit View Zoom Library Run Reports Tools Help

Project: PCIE

- IBIS diff_out
 - Structure
 - Validating
- IBIS diff_out_emp
 - Structure
 - Validating
- M Model1
 - Structure
 - Validating
- M HSpice
 - Structure
 - Validating

Properties

Subcircuits

X1

| | |
|------|----------|
| Name | X1 |
| tcyc | 1000e-12 |

X2

| | |
|------|----------|
| Name | X2 |
| tcyc | 1000e-12 |

Buffers

U1.1(+),U1.1(-)

Reference Nar U1

| | |
|----------|----|
| Power | On |
| pu_scal | 1 |
| pd_scal | 1 |
| pc_scal | 1 |
| gc_scal | 1 |
| c_com_pu | NA |
| c_com_pd | NA |
| c_com_pc | NA |
| c_com_gc | NA |
| rwf_scal | 1 |
| fwf_scal | 1 |

U2.3(+),U2.3(-)

Reference Nar U2

| | |
|----------|----|
| Power | On |
| pu_scal | 1 |
| pd_scal | 1 |
| pc_scal | 1 |
| gc_scal | 1 |
| c_com_pu | NA |
| c_com_pd | NA |
| c_com_pc | NA |
| c_com_gc | NA |
| rwf_scal | 1 |
| fwf_scal | 1 |

Pins

| | |
|------|------|
| Name | inp |
| Name | inn |
| Name | outp |
| Name | outn |

Structure Fitting Validating

BU1.1 node33 node34 outp inp node37 node38 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.ibs' model='diff_out_p' Power=On pu_scal=1 pd_scal=1 pc_scal=1 gc_scal=1 rwf_scal=1 fwf_scal=1

BU1.2 node39 node40 outn inn node43 node44 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.ibs' model='diff_out_n' Power=On pu_scal=1 pd_scal=1 pc_scal=1 gc_scal=1 rwf_scal=1 fwf_scal=1

BU2.3 node13 node14 outp node31 node17 node18 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.ibs' model='diff_out_emp_p' Power=On pu_scal=1 pd_scal=1 pc_scal=1 gc_scal=1 rwf_scal=1 fwf_scal=1

BU2.4 node19 node20 outn node29 node23 node24 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.ibs' model='diff_out_emp_n' Power=On pu_scal=1 pd_scal=1 pc_scal=1 gc_scal=1 rwf_scal=1 fwf_scal=1

X1 node31 inp GND DELAY_CKT tcyc=1000e-12

X2 node29 inn GND DELAY_CKT tcyc=1000e-12

Project Library HSpice

Ready

NUM

Fitting for Accuracy

The screenshot displays the SIMDE V1.0 software interface. The main window shows a circuit diagram with a voltage source V1, a resistor R1 (100ohm), and a subcircuit X1 (Model1.mdl). A differential voltage probe is connected to the output nodes. The bottom status bar indicates the project is 'Ready' and the simulation is 'HSpice'.

The **Fitting Report - Model: Model1** window is open, showing a table of fitting results for 14 data points. The table includes columns for ID, Probe, DAI(%), DPI(%), DA, DP, \$pu1, and \$pu2. The values for \$pu1 and \$pu2 are highlighted in red for the 9th data point.

| ID | Probe | DAI(%) | DPI(%) | DA | DP | \$pu1 | \$pu2 |
|----|--------|--------|--------|------|------|-------|-------|
| 0 | probe1 | 9.34 | 34.75 | 0.05 | 0.19 | 0.6 | 0.95 |
| 1 | probe1 | 9.47 | 42.28 | 0.05 | 0.23 | 1.5 | 0.95 |
| 2 | probe1 | 5.42 | 38.15 | 0.03 | 0.21 | 0.96 | 0.95 |
| 3 | probe1 | 6.74 | 36.82 | 0.04 | 0.20 | 816m | 0.95 |
| 4 | probe1 | 5.90 | 37.54 | 0.03 | 0.20 | 902m | 0.95 |
| 5 | probe1 | 5.61 | 37.91 | 0.03 | 0.20 | 937m | 0.95 |
| 6 | probe1 | 5.47 | 38.05 | 0.03 | 0.20 | 951m | 0.95 |
| 7 | probe1 | 12.70 | 34.98 | 0.07 | 0.19 | 0.96 | 0.4 |
| 8 | probe1 | 9.38 | 40.30 | 0.05 | 0.22 | 0.96 | 1.5 |
| 9 | probe1 | 5.20 | 38.54 | 0.03 | 0.21 | 0.96 | 1.06 |
| 10 | probe1 | 6.98 | 39.37 | 0.04 | 0.21 | 0.96 | 1.24 |
| 11 | probe1 | 5.92 | 38.78 | 0.03 | 0.21 | 0.96 | 1.13 |
| 12 | probe1 | 5.55 | 38.64 | 0.03 | 0.21 | 0.96 | 1.09 |
| 13 | probe1 | 5.29 | 38.58 | 0.03 | 0.21 | 0.96 | 1.07 |

The **Parameter editor** window is also open, showing the following parameters:

| Name | Value | Start | Stop | Step |
|-------|-------|-------|------|------|
| \$pu1 | 0.6 | 0.6 | 1.5 | |
| \$pu2 | 0.4 | 0.4 | 1.5 | |

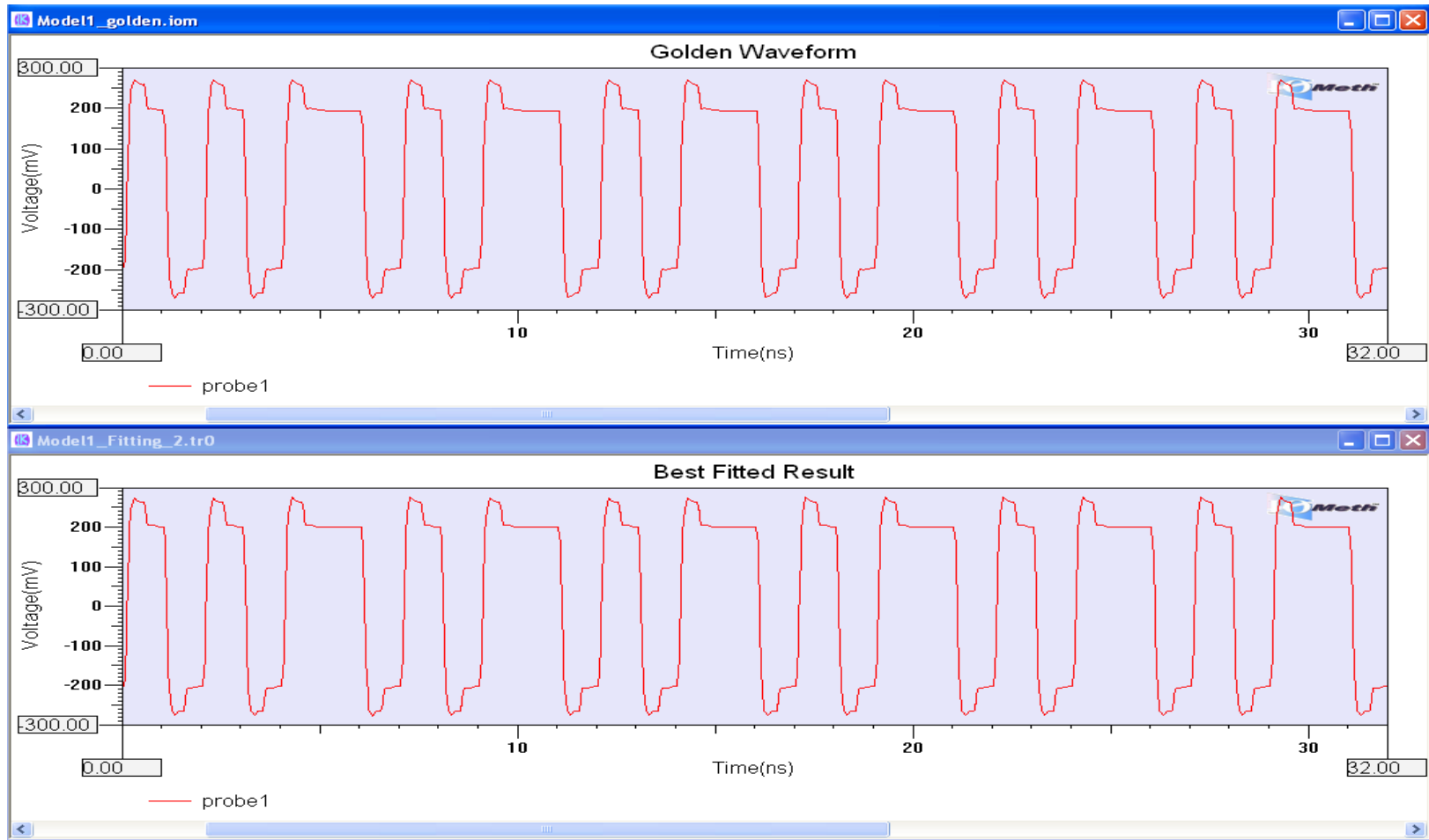
The **Structure** tab is selected, showing the following components:

- X1 node1 node2 node7 node8 Model1 pu1=pu1 pu2=pu2
- R1 node7 node8 R=100
- V1.+ node1 GND CUSTOMISED
- V1.- node2 GND CUSTOMISED

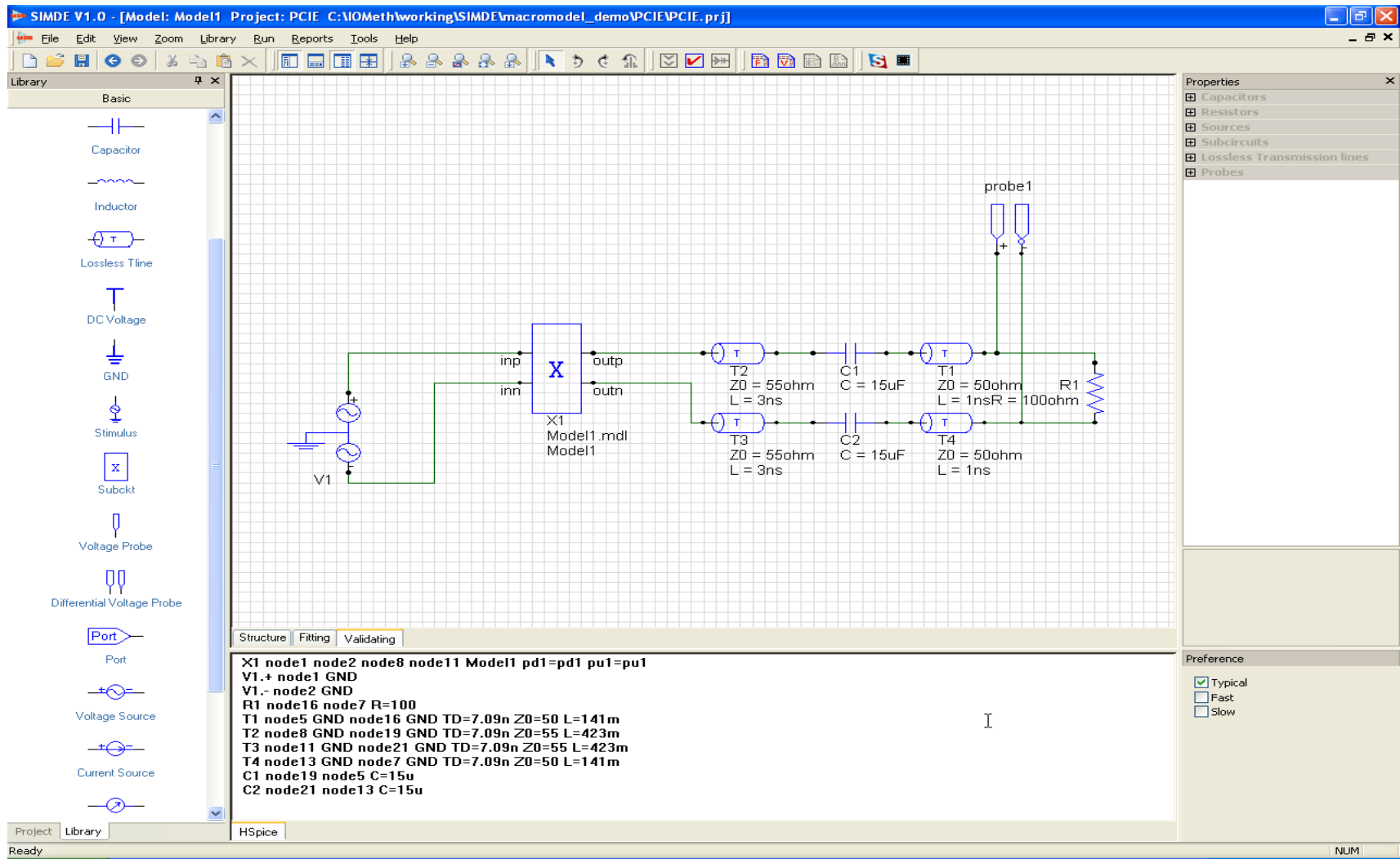
The **Preference** window is also open, showing the following options:

- ☒ Typical
- ☐ Fast
- ☐ Slow

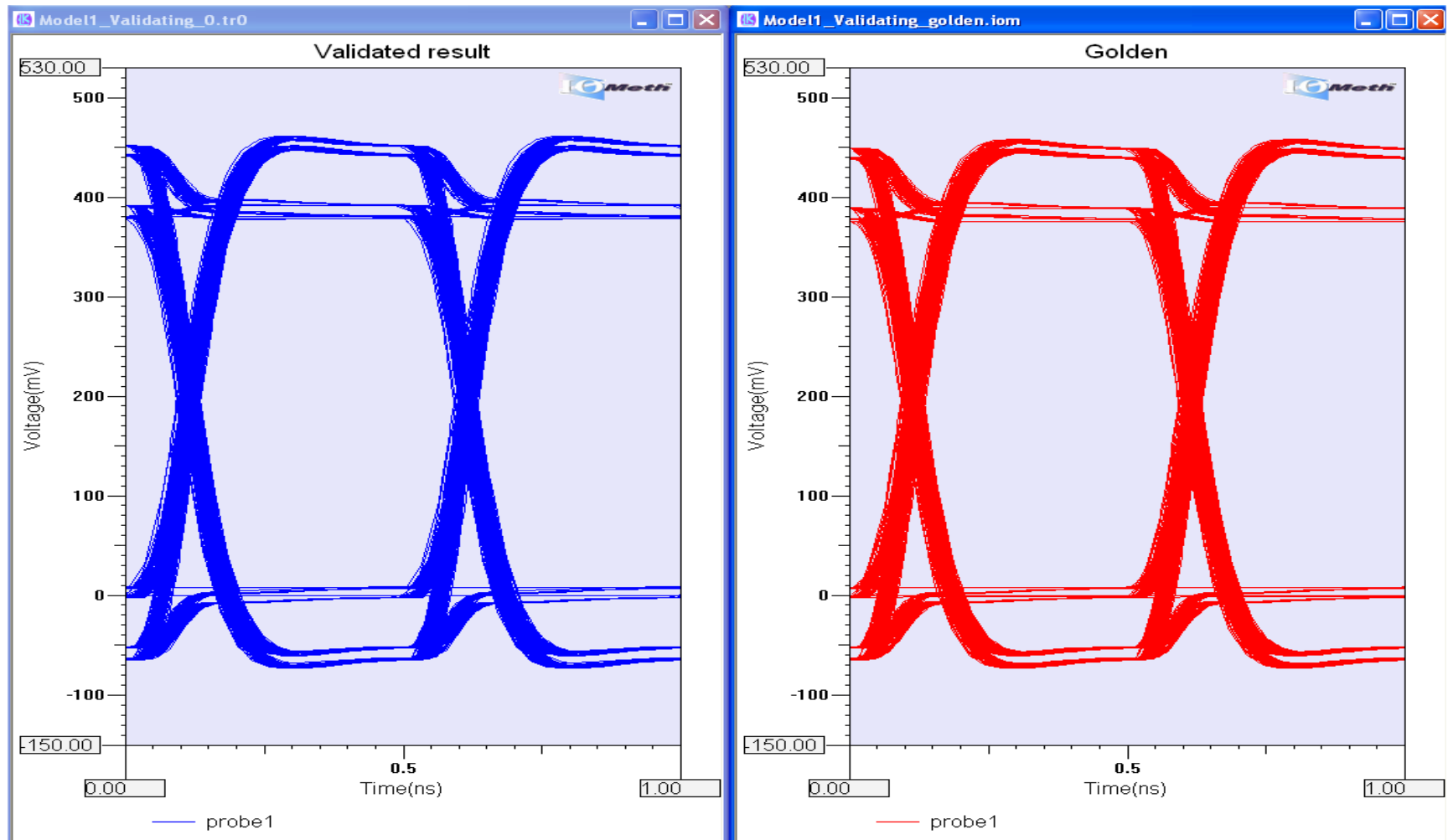
Fitting Result (DPI:1.14%, DAI:1.49%)



Free-Form Topology Editor for Validation



Validation Result



The Modeling Specialist



<http://www.iometh.com>